11-6625-3031-14

TM 11-6625-3031-14

TECHNICAL MANUAL

# OPERATOR'S, ORGANIZATIONAL,
# DIRECT SUPPORT,
# AND
# GENERAL SUPPORT MAINTENANCE MANUAL

# COUNTER, PULSE, ELECTRONIC
# TD-1338(V)1/USM
## (NSN 6625-01-120-7832)

HEADQUARTERS, DEPARTMENT OF THE ARMY

0101.11:

6 MAY 1983

READEX FICHE best copy available

# SAFETY STEPS TO FOLLOW IF SOMEONE IS THE VICTIM OF ELECTRICAL SHOCK

① DO NOT TRY TO PULL OR GRAB THE INDIVIDUAL

② IF POSSIBLE, TURN OFF THE ELECTRICAL POWER

③ IF YOU CANNOT TURN OFF THE ELECTRICAL POWER, PULL, PUSH, OR LIFT THE PERSON TO SAFETY USING A WOODEN POLE OR A ROPE OR SOME OTHER INSULATING MATERIAL

④ SEND FOR HELP AS SOON AS POSSIBLE

⑤ AFTER THE INJURED PERSON IS FREE OF CONTACT WITH THE SOURCE OF ELECTRICAL SHOCK, MOVE THE PERSON A SHORT DISTANCE AWAY AND IMMEDIATELY START ARTIFICIAL RESUSCITATION

TECHNICAL MANUAL
NO. 11-6625-3031-14

HEADQUARTERS
DEPARTMENT OF THE ARMY
WASHINGTON, D.C. 6 May 1983

# OPERATOR'S, ORGANIZATIONAL, DIRECT SUPPORT AND GENERAL SUPPORT MAINTENANCE MANUAL

## FOR

# COUNTER, PULSE, ELECTRONIC

## TD-1338(V)1/USM

## (NSN 6625-01-120-7832)

### REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in the back of this manual direct to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: DRSEL-ME-MP, Fort Monmouth, NJ 07703.

In either case, a reply will be furnished direct to you.

## TABLE OF CONTENTS

| | | | Para | Page |
|---|---|---|---|---|
| Chapter | 1. | INTRODUCTION | | |
| Section | I. | General Information | | 1-1 |
| | | Scope | 1-1 | 1-1 |
| | | Reports of maintenance forms, records and reports | 1-2 | 1-1 |
| | | Administrative storage | 1-3 | 1-1 |
| | | Destruction of Army electronics materiel. | 1-4 | 1-1 |
| | | Reporting equipment improvement recommendations (EIR's) | 1-5 | 1-1 |
| | | Warranty information | 1-6 | 1-1 |
| | II. | Equipment Description | | 1-2 |
| | | Equipment characteristics, capabilities and features | 1-7 | 1-2 |
| | | Equipment data | 1-8 | 1-2 |
| | III. | Technical Principles of Operation | | 1-4 |
| | | Counter functional operation | 1-9 | 1-4 |

TABLE OF CONTENTS - Continued

| | | | Para | Page |
|---|---|---|---|---|
| | | Basic counter A1 | 1-10 | 1-6 |
| | | Converter A2 | 1-11 | 1-8 |
| Chapter | 2. | OPERATING INSTRUCTIONS | | |
| Section | I. | Description and Use of Operator's Controls and Indicators | | 2-1 |
| | | Front-panel controls, connectors and indicators | 2-1 | 2-1 |
| | | Rear-panel controls and connectors | 2-2 | 2-1 |
| | II. | Preventive Maintenance Checks and Services | | 2-5 |
| | | General instructions | 2-3 | 2-5 |
| | | PMCS procedures | 2-4 | 2-5 |
| | | Cleaning instructions | 2-5 | 2-6 |
| | III. | Operation Under Usual Conditions | | 2-7 |
| | | Assembly and preparation for use | 2-6 | 2-7 |
| | | Operation as stand-alone instrument | 2-7 | 2-8 |
| | | Externally enabled operation | 2-8 | 2-10 |
| | | Pulse profile measurements | 2-9 | 2-10 |
| | | Dynamic characteristics of time varying signals | 2-10 | 2-11 |
| | | Multiple pulse signal measurements | 2-11 | 2-11 |
| | | Timing considerations | 2-12 | 2-11 |
| | | Accuracy | 2-13 | 2-12 |
| | | Techniques for improving accuracy | 2-14 | 2-13 |
| | | Operation using General Purpose Interface Bus | 2-15 | 2-13 |
| Chapter | 3. | OPERATOR AND ORGANIZATIONAL MAINTENANCE | | |
| Section | I. | Lubrication | | 3-1 |
| | II. | Troubleshooting Procedures | | 3-1 |
| | III. | Maintenance Procedures | | 3-3 |
| | | Introduction | 3-4 | 3-3 |
| | | Inspection | 3-5 | 3-3 |
| | | Cleaning | 3-6 | 3-3 |
| | | Replacement | 3-7 | 3-3 |
| | | Test | 3-8 | 3-3 |
| Chapter | 4. | DIRECT SUPPORT AND GENERAL SUPPORT MAINTENANCE | | |
| Section | I. | Repair Parts, Special Tools; Test Measurement, and Diagnostic Equipment (TMDE); and Support Equipment | | 4-1 |
| | | Common tools and equipment | 4-1 | 4-1 |
| | | Special tools, TMDE, and support equipment | 4-2 | 4-1 |
| | | Repair parts | 4-3 | 4-1 |
| | II. | Service Upon Receipt | | 4-1 |
| | III. | Troubleshooting | | 4-1 |
| | | Introduction | 4-5 | 4-1 |
| | | Reference diagrams | 4-6 | 4-2 |
| | IV. | Maintenance Procedures | | 4-17 |
| | | Disassembly, replacement, and reassembly | 4-7 | 4-17 |
| | | Adjustments | 4-8 | 4-20 |
| | | Performance test | 4-9 | 4-28 |

TABLE OF CONTENTS - Continued

| | | | Para | Page |
|---|---|---|---|---|
| Section | V. | Preparation for Storage or Shipment | | 4-33 |
| | | Preparation of equipment | 4-10 | 4-33 |
| | | Packing instructions | 4-11 | 4-33 |
| Appendix | A. | REFERENCES | | A-1 |
| Appendix | B. | MAINTENANCE ALLOCATION | | B-1 |
| Appendix | C. | COMPONENTS OF END ITEM AND BASIC ISSUE ITEMS LISTS | | C-1 |
| Appendix | D. | ADDITIONAL AUTHORIZATION LIST | | D-1 |
| Appendix | E. | EXPENDABLE SUPPLIES AND MATERIALS LIST | | E-1 |

## LIST OF ILLUSTRATIONS

| Figure | Title | Page |
|---|---|---|
| 1-1 | Counter, Pulse, Electronic TD-1338(V)1/USM | 1-0 |
| 1-2 | Counter, Functional Block Diagram. | 1-5 |
| 1-3 | Basic Counter A1, Functional Block Diagram | 1-7 |
| 1-4 | Converter A2, Functional Block Diagram | 1-9 |
| 2-1 | Counter Front Panel. | 2-1 |
| 2-2 | Counter Rear Panel | 2-4 |
| 2-3 | Pulse Profile Measurement Test Setup | 2-10 |
| 2-4 | Pulse Profile Measurement | 2-10 |
| 2-5 | Time Varying Signal Measurement Test Setup | 2-11 |
| 2-6 | Internal Timing Delays | 2-12 |
| 2-7 | GPIB Capabilities and Structure | 2-15 |
| 2-8 | GPIB IEEE STD 488/1975 ADDRESS SWITCH Positions | 2-16 |
| 4-1 | Subassembly and Cable Locations | 4-3 |
| 4-2 | Counter Interconnect A100, Connector and Switch Locations | 4-17 |
| 4-3 | Counter, Partial Exploded View | 4-18 |
| 4-4 | Adjustment Locations | 4-21 |
| 4-5 | Pulse Generator Output | 4-23 |
| 4-6 | YIG Control A202, Adjustment and Test Point Locations | 4-24 |
| 4-7 | Detected Modulation and 20 kHz Reference Pulse Timing | 4-24 |
| 4-8 | Converter Sequencer A203, Adjustment and Test Point Locations. | 4-26 |
| 4-9 | Return Loss Measurement Setup | 4-26 |
| 4-10 | Return Loss Measurement Waveform | 4-27 |
| 4-11 | Typical Attenuator Control Ramp Offset | 4-27 |
| 4-12 | Comb Line | 4-27 |
| FO-1 | Counter Interconnection Schematic Diagram | |
| FO-2 | Interconnection Diagram, Detailed Technical Schematic | |
| FO-3A | Component Locator Counter Interconnect (A100) | |
| FO-3B | Schematic Diagram Counter Interconnect (A100) | |
| FO-4A | Component Locator and Descriptive Information Count Chain Control (A102) | |
| FO-4B | Schematic Diagram Count Chain Control (A102) | |
| FO-5A | Component Locator and Descriptive Information Count Chain (A103) | |
| FO-5B | Schematic Diagram Count Chain (A103) | |
| FO-6A | Component Locator and Descriptive Information Control (A104) | |
| FO-6B | Schematic Diagram Control (A104) | |
| FO-7A | Component Locator and Descriptive Information Gate Generator (A105) | |
| FO-7B | Schematic Diagram Gate Generator (A105) | |
| FO-8A | Component Locator and Descriptive Information High Frequency (A106) | |
| FO-8B | Schematic Diagram High Frequency (A106) | |
| FO-9A | Component Locator and Descriptive Information Power Supply (A107) | |
| FO-9B | Schematic Diagram Power Supply (A107) | |
| FO-10A | Component Locator and Descriptive Information Reference Oscillator Buffer (A108) | |
| FO-10B | Schematic Diagram Reference Oscillator Buffer (A108) | |

## LIST OF ILLUSTRATIONS (Continued)

| Figure | Title |
|---|---|
| FO-11A | Component Locator and Descriptive Information Display (A110) |
| FO-11B | Schematic Diagram Display (A110) |
| FO-12A | Component Locator Converter Interconnect (A200) |
| FO-12B | Schematic Diagram Converter Interconnect (A200) |
| FO-13A | Component Locator and Descriptive Information Source/Amplifier (A201) |
| FO-13B | Schematic Diagram Source/Amplifier (A201) |
| FO-14A | Component Locator and Descriptive Information Yig Control (A202) |
| FO-14B | Schematic Diagram Yig Control (A202) |
| FO-15A | Component Locator and Descriptive Information Converter Sequencer (A203) |
| FO-15B | Schematic Diagram Converter Sequencer (A203) |
| FO-16A | Component Locator and Descriptive Information IF Processor (A204) |
| FO-16B | Schematic Diagram IF Processor (A204) |

## LIST OF TABLES

| Table | Title | Page |
|---|---|---|
| 1-1 | Specifications | 1-1 |
| 2-1 | Front-panel Controls, Connectors and Indicators | 2-1 |
| 2-2 | Rear-panel Controls and Connectors | 2-5 |
| 2-3 | Operator Preventive Maintenance Checks and Services | 2-6 |
| 2-4 | Counter GPIB Capability Identification Codes | 2-14 |
| 2-5 | GPIB IEEE STD 488/1975 Connector Pin Assignments | 2-16 |
| 2-6 | On Line and Off Line ADDRESS SWITCH Settings | 2-17 |
| 2-7 | ADDRESS SWITCH Settings vs ASCII Characters | 2-18 |
| 2-8 | Programming Summary | 2-20 |
| 2-9 | Typical Program Using Hewlett-Packard 9815 Calculator as Controller | 2-26 |
| 3-1 | Operator and Organizational Troubleshooting | 3-1 |
| 4-1 | Symptom Index | 4-2 |
| 4-2 | Direct Support and General Support Troubleshooting | 4-4 |
| 4-3 | Power Supply Voltages and Adjustments | 4-22 |
| 4-4 | Band B Response Tests | 4-29 |
| 4-5 | Preset Frequency Tests | 4-31 |
| 4-6 | Control Sequence | 4-45 |
| 4-7 | Converter Sequence Functions | 4-65 |

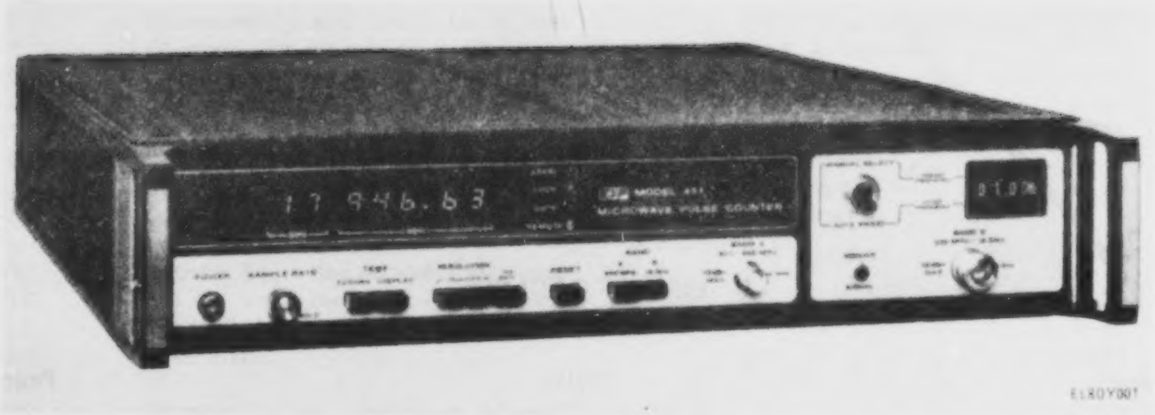

17 946.63
MICROWAVE PULSE COUNTER
EL8OY001

Figure 1-1. Counter, Pulse, Electronic TD-1338(V)1/USM

# CHAPTER 1
# INTRODUCTION

## Section I. GENERAL INFORMATION

### 1-1. Scope.

a. This technical manual covers operation and maintenance of Counter, Pulse, Electronic TD-1338(V)1/USM. Throughout this manual it is referred to as the counter.

b. The counter (fig. 1-1) is used to measure the frequency of cw, pulse-modulated, or frequency-modulated microwave signals between 300 MHz and 18 GHz. Pulse widths can be as narrow as 100 nanoseconds, with a maximum pulse repetition frequency of 2.5 MHz. Peak-to-peak deviation of FM signals may be as great as 40 MHz at 10 MHz modulation rates.

### 1-2. Reports of Maintenance Forms, Records and Reports.

a. Reports of Maintenance and Unsatisfactory Equipment. Department of the Army forms and procedures used for equipment maintenance will be those prescribed by TM 38-750, The Army Maintenance Management System (Army). Air Force personnel will use AFM 66-1 for maintenance reporting and TO 00-35D54 for unsatisfactory equipment reporting.

b. Report of Packaging and Handling Deficiencies. Fill out and forward SF 364 (Report of Discrepancy (ROD)) as prescribed in AR 735-11-2/DLAR 4140.55/NAVMATINST 4355.73/AFR 400-54/MCO 4430.3E.

c. Discrepancy in Shipment Record (DISREP) (SF 361). Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33B/AFR 75-18/MCO P4610.19C/DLAR 4500.15.

### 1-3. Administrative Storage.

Administrative storage of equipment issued to and used by Army activities will have preventive maintenance performed in accordance with the PMCS charts before storing. When removing the equipment from administrative storage, the PMCS should be performed to assure operational readiness.

### 1-4. Destruction of Army Electronics Materiel.

Destruction of Army electronics materiel to prevent enemy use shall be in accordance with TM 750-244-2.

### 1-5. Reporting Equipment Improvement Recommendations (EIR's).

If your counter needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment. Let us know why you don't like the design or performance. Put it on an SF 368 (Quality Deficiency Report). Mail it to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: DRSEL-ME-MP, Fort Monmouth, New Jersey 07703. We'll send you a reply.

### 1-6. Warranty Information.

The counter is warranted by EIP Microwave, Inc. for 12 months. It starts on the date, found in block 23, DA Form 2408-9, in the logbook. Report all defects in material or workmanship to your supervisor, who will take appropriate action through your organizational maintenance shop.

## Section II. EQUIPMENT DESCRIPTION

### 1-7. Equipment Characteristics, Capabilities and Features.

The counter is a portable test instrument usable as either self-contained frequency measurement or monitoring indicator, or as part of a programmable automatic test equipment (ATE) system. It provides a direct readout of frequency from 300 MHz through 18 MHz. Capabilities and features include:

a. Measures pulse-modulated microwave signals.
b. Measures frequency-modulated microwave signals.
c. Measures cw microwave signals.
d. Front panel self-test of digital display.
e. Front panel self-test of internal circuits.
f. Automatic and selectable resolution of readout display.
g. Overload protection built in at input connector.
h. Simple change to cover different power line voltages.
i. Front-panel selection of frequency scanning limits.
j. Compatable with IEEE STD 488 General Purpose Interface Bus (GPIB).

### 1-8. Equipment Data.

Table 1-1 lists the electrical and physical characteristics of the counter.

Table 1-1. Specifications

| | | |
|---|---|---|
| Frequency Range: | | |
| Band A | 300 MHz to 950 MHz | |
| Band B | 925 MHz to 18 GHz | |
| Pulse Characteristics: | | |
| Pulse width | 100 nsec min, measured at 3-dB points | |
| Pulse repetition frequency | Minimum 50 Hz or 0 Hz, rear panel selectable. Maximum 2.5 MHz. Minimum time between pulses 300 nsec. | |
| Accuracy: | | |
| CW or pulse > 100 μsec | Time base accuracy ± 1 count | |
| Pulse < 100 μsec | Time base accuracy ± averaging error ± gate error | |
| Averaging Error (kHz rms): | Band A | Band B |
| 100 μsec gate | $\frac{200}{\sqrt{PW - 0.03}}$ | $\frac{100}{\sqrt{PW - 0.03}}$ |
| 1 msec gate | $\frac{60}{\sqrt{PW - 0.03}}$ | $\frac{30}{\sqrt{PW - 0.03}}$ |
| Gate error (max) | $\frac{\pm 100 \text{ kHz}}{PW - 0.03}$ | $\frac{\pm 40 \text{ kHz}}{PW - 0.03}$ |

NOTE

PW = pulse width in μsec

### Table 1-1. Specifications - Continued

| | | |
|---|---|---|
| Time Base: | Temperature compensated crystal oscillator (TCXO) | |
| Crystal frequency | 10 MHz | |
| Stability: | | |
| Aging rate | $<\|3 \times 10^{-7}\|$ per month | |
| Temperature | $<\|2 \times 10^{-6}\|$, 0 to 50°C | |
| Line voltage | $<\|1 \times 10^{-7}\|$ for ±10% change | |
| Sensitivity | Band A | Band B |
| | 300 - 950 MHz:<br>-10 dBm peak | 925 MHz - 10 GHz:<br>-10 dBm peak<br>10 GHz - 18 GHz:<br>-5 dBm peak |
| Input Impedance | 50 ohms nominal | 50 ohms nominal |
| Connector Types | BNC | N (precision) |
| Maximum Input Peak Level: | | |
| Operating | +10 dBm | +10 dBm |
| Burnout level | +27 dBm | +30 dBm |
| Reading Time (sec): | | |
| 100 μsec gate | $\frac{400}{(PW)(PRF)}$ | $\frac{100}{(PW)(PRF)}$ |
| 1 msec gate | $\frac{4000}{(PW)(PRF)}$ | $\frac{1000}{(PW)(PRF)}$ |

NOTE

PW = pulse width in μsec

PRF = pulse repetition frequency in Hertz

| | |
|---|---|
| Display | 7-digit light emitting diode (LED)<br>Fixed decimal point<br>Leading zero suppression |
| Band B Minimum FM Tolerance: | |
| CW | 40 MHz p-p deviation for modulation rates dc to 10 MHz |
| Pulse | Without input inhibit: 20 MHz maximum frequency shift across pulse |
| Frequency profile | With input inhibit: 20 MHz maximum frequency shift during input inhibit pulse |

Table 1-1. Specifications - Continued

| | |
|---|---|
| Band B Acquisition Time: | |
| PRF > 100 Hz | 100 msec + 50 msec/GHz |
| PRF < 100 Hz | 100 msec + $\frac{5}{PRF}$ sec/GHz |
| Resolution | 10 kHz, 100 kHz, 1 MHz |
| General Purpose Interface Bus (GPIB) | IEEE Standard Digital Interface for Programmable Instrumentation, IEEE STD 488-1975 |
| Power | 115 or 230 Vac ± 10%, 50/60 Hz;<br>115 Vac ± 10%, 400 Hz; single phase;<br>100 watts nominal |
| Operating Temperature | 0 - 50°C |
| Warm up Time | None Required |
| Weight | 30 lb |
| Dimensions (inches) | 3.5 H x 16.75 W x 19.0 D |

## Section III. TECHNICAL PRINCIPLES OF OPERATION

### 1-9. Counter Functional Operation. (Fig. 1-2.)

a. The counter automatically measures and displays the frequency of cw or pulse-modulated signals from 300 MHz through 18 GHz. With accessory equipment, the counter can make dynamic frequency measurements; measurement windows as narrow as 20 nanoseconds are possible. Two primary input connectors on the front panel, BAND A 300 - 950 MHz and BAND B 925 MHz - 18 GHz, are used to connect the counter to the external frequency source. An auxiliary INPUT INHIBIT connector on the rear panel can be used to control the time during which an actual reading is made. Control of the counter can be accomplished by front-panel switches or by a General Purpose Interface Bus (GPIB) from an external GPIB controller. The output of the counter is displayed on a 7-digit, fixed decimal, light emitting diode (LED) display and can be transmitted through the GPIB for other purposes. Accuracy of the counter is controlled by Reference Oscillator Buffer A108 with outputs to Basic Counter A1 and Converter A2; a third output is connected to a rear-panel 10 MHz OUTPUT connector.

b. Band A signals are fed into a divide-by-four circuit in Prescaler A109, whose output is directed to Basic Counter A1 through Dual Delay Line A116. The divide-by-four frequency is counted in the basic counter for either a 400 microsecond or 4 millisecond period to obtain 10 kHz resolution readout on Display A110. The counter gate in A1 is enabled by the input signal and is open only when a signal is present.

c. Band B signals are fed into Converter A2, converted to an IF signal by heterodyning the input signal against a 200 MHz harmonic, and directed to A1 through Delay Line A112. The counter gate in A1 is enabled by the input signal and is open only when a signal is present. In A1, resolution is inversely proportional to the measurement

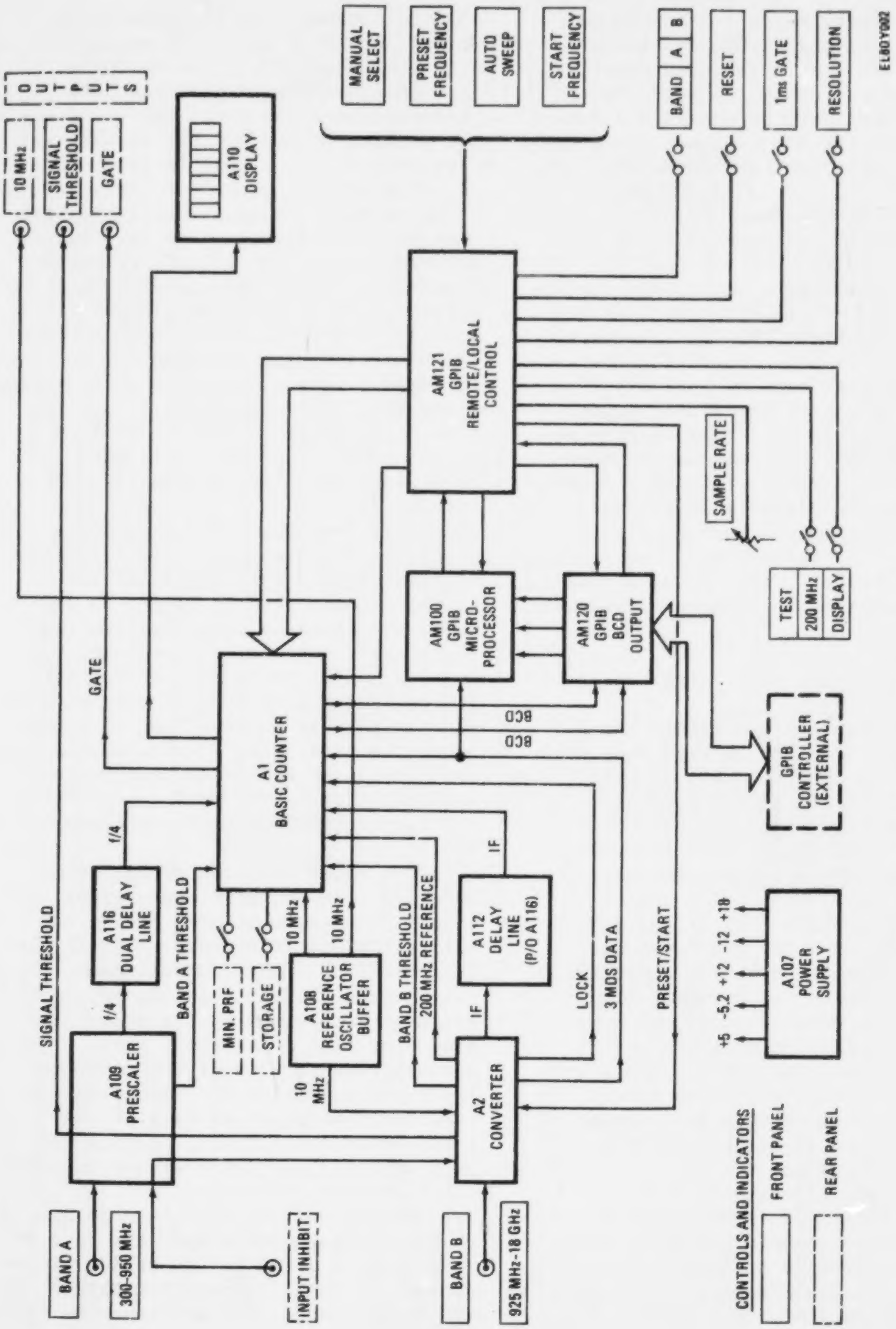

BAND A
300-950 MHz
INPUT INHIBIT
BAND B
925 MHz-18 GHz
A109 PRESCALER
A116 DUAL DELAY LINE
f/4
f/4
SIGNAL THRESHOLD
BAND A THRESHOLD
GATE
A1 BASIC COUNTER
MIN. PRF
STORAGE
A108 REFERENCE OSCILLATOR BUFFER
10 MHz
10 MHz
10 MHz
BAND B THRESHOLD
200 MHz REFERENCE
A2 CONVERTER
IF
A112 DELAY LINE (P/O A116)
IF
LOCK
3 MDS DATA
PRESET/START
BCD
BCD
AM100 GPIB MICRO-PROCESSOR
AM120 GPIB BCD OUTPUT
AM121 GPIB REMOTE/LOCAL CONTROL
GPIB CONTROLLER (EXTERNAL)
A110 DISPLAY
10 MHz
SIGNAL THRESHOLD
GATE
OUTPUTS
MANUAL SELECT
PRESET FREQUENCY
AUTO SWEEP
START FREQUENCY
BAND A B
RESET
1ms GATE
RESOLUTION
SAMPLE RATE
TEST
200 MHz
DISPLAY
A107 POWER SUPPLY
+5 -5.2 +12 -12 +18
CONTROLS AND INDICATORS
FRONT PANEL
REAR PANEL
EL8OY002

Figure 1-2. Counter, Functional Block Diagram

time. For example: a 1 microsecond gate time will give 1 MHz resolution. To get 10 kHz resolution, the counter automatically averages as many input pulses as necessary to obtain a total gate time of 100 microseconds or 1 millisecond. The required number of pulses is a function of input pulse width. The intermediate frequency from A2 is processed and counted in A1 and displayed on A110.

d. Three rear-panel connectors provide 10 MHz, SIGNAL THRESHOLD, and GATE OUTPUTS. The 10 MHz OUTPUT is a service convenience for adjusting the temperature compensated crystal oscillator (TCXO) on Reference Oscillator Buffer A108. The other two signal outputs may be used for dynamic frequency measurements such as pulse profile measurements or time varying signal measurements.

e. Power Supply A107 provides +5, -5.2, +12, -12, and +18 volts dc for the counter circuits. The +18 Vdc output is unregulated; the other four voltages are regulated.

## 1-10. Basic Counter A1. (Fig. 1-3.)

a. Input signals from either the low range (300 - 950 MHz) or high range (925 MHz - 18 GHz) sources, or both, are applied to the signal processor circuits on High Frequency Circuit Card A106. The signal from Prescaler A109 is the BAND A input frequency, divided by four (f/4). The signal from I.F. Processor A204 is the BAND B input frequency minus the reference frequency identified as the converter IF signal. Selection of which signal to display is controlled by the front panel BAND selection switches or by GPIB selection. Only one of the signal inputs can be displayed even though both may be connected to the counter. The f/4 and the IF signal inputs are 360 MHz or lower and are directed to the 400 MHz decade circuits on A106.

b. Two threshold (Band A and/or Band B) control levels are applied to Gate Generator A105 to provide a gate output to the 400 MHz decade through the gate calibrator. The Band A threshold comes from Prescaler A109 while the Band B threshold comes from I.F. Processor A204 in Converter A2.

c. When an input signal has been processed into the range below 360 MHz and applied to the 400 MHz decade, the frequency of the signal is determined by accumulating the number of signal cycles occuring within a precisely determined time interval (gate). The gate period is dependent on the 200 MHz reference frequency. Total time intervals of the gates are 100 microseconds and 1 millisecond for Band B, or 400 microseconds and 4 milliseconds for Band A. In order to measure narrow pulses to a resolution of 10 kHz, it is necessary to add the number of cycles counted in each of a large number of pulses until the required total time interval is obtained.

d. Gate Generator A105 provides a precision interval gate. This function is considerably more difficult for pulsed signals than it is for cw signals, and it is on this function that the overall accuracy of the counter depends. A105 performs two functions; it supplies a gate to A106 only when an input signal is present, and it accumulates the total time of gate application for periods of either 100 microseconds or 1 millisecond for Band B, or either 400 microseconds or 4 milliseconds for Band A.

e. The first function or operation requires that the gate begin after the signal is present at A106 and to end before the end of signal. This is done by generating a gate approximately 30 nanoseconds shorter than the RF signal start as determined by the associated Band A or Band B threshold level. The arrival time at A106 of the converter IF or the prescaler f/4 signal is controlled by delay lines in A116, in series with the signals, so that the gate will fall entirely within the signal pulse application.

f. The second function is done by counting clock pulses when the gate is open until a total period of 100 microseconds or 1 millisecond for Band B, or 400 microseconds or 4 milliseconds for

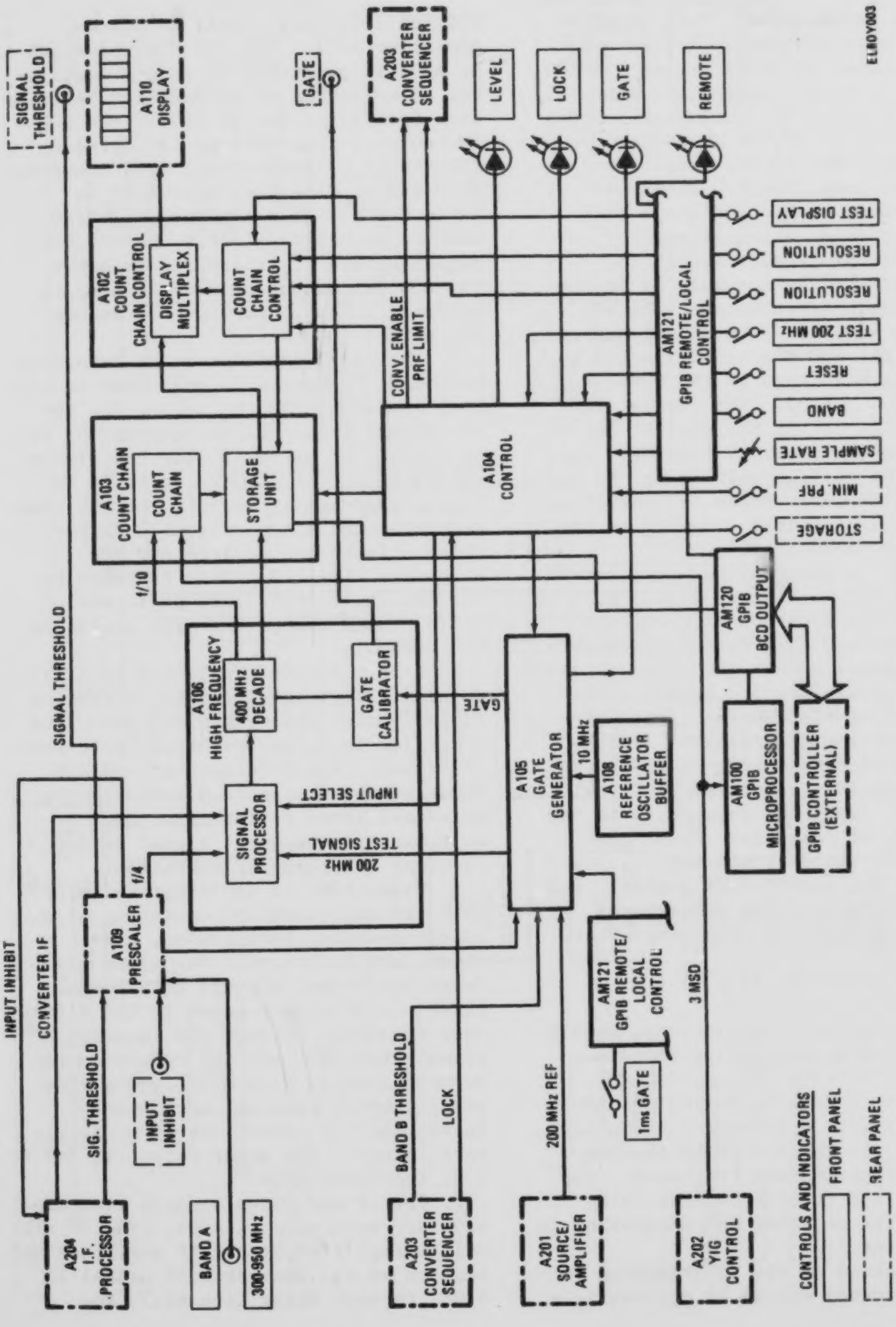

A204 I.F. PROCESSOR
INPUT INHIBIT
CONVERTER IF
SIG. THRESHOLD
SIGNAL THRESHOLD
SIGNAL THRESHOLD
A110 DISPLAY
INPUT INHIBIT
A109 PRESCALER
f/4
BAND A
300-950 MHz
A106 HIGH FREQUENCY
SIGNAL PROCESSOR
400 MHz DECADE
GATE CALIBRATOR
200 MHz TEST SIGNAL
INPUT SELECT
GATE
1/10
A103 COUNT CHAIN
COUNT CHAIN
STORAGE UNIT
A102 COUNT CHAIN CONTROL
DISPLAY MULTIPLEX
COUNT CHAIN CONTROL
GATE
A203 CONVERTER SEQUENCER
BAND B THRESHOLD
LOCK
CONV. ENABLE
PRF LIMIT
A104 CONTROL
A201 SOURCE/ AMPLIFIER
200 MHz REF
A105 GATE GENERATOR
10 MHz
A108 REFERENCE OSCILLATOR BUFFER
AM121 GPIB REMOTE/ LOCAL CONTROL
1ms GATE
LEVEL
LOCK
GATE
REMOTE
AM121 GPIB REMOTE/LOCAL CONTROL
A202 YIG CONTROL
3 MSD
AM120 GPIB BCD OUTPUT
AM100 GPIB MICROPROCESSOR
GPIB CONTROLLER (EXTERNAL)
TEST DISPLAY
RESOLUTION
RESOLUTION
TEST 200 MHz
RESET
BAND
SAMPLE RATE
MIN. PRF
STORAGE
CONTROLS AND INDICATORS
FRONT PANEL
REAR PANEL
ELNOY003

Figure 1-3. Basic Counter A1, Functional Block Diagram

Band A, is accumulated. This requires that each gate opening is for an exact integral number of clock pulses. A 200 MHz clock is used, causing the gate width to increase in 5 nanosecond steps until a total of 20,000 steps for 100 microseconds, 80,000 steps for 400 microseconds, 200,000 steps for 1 millisecond, or 800,000 steps for 4 milliseconds is accumulated.

g. The signal passes through the counter gate and is accumulated in the counting-chain first decade, the 400 MHz decade on A106. The signal output (f/10) of the 400 MHz decade is fed to the storage unit through the 6-decade count chain of A103. The storage unit on A103 holds all of the digital information from the previous reading. Output from the storage unit is fed to the display multiplexer which is controlled by count chain control circuits on the Count Chain Control A102.

h. Output of the display multiplexer on A102 is fed to Display A110. A110 is mounted on the front panel along with LEVEL, LOCK, and GATE status indicators. The front-panel REMOTE indicator is used with GPIB controller operations. Overall control of the counter is performed by Control Circuit Card A104. Front-panel selection switching is routed to A104 through GPIB Remote/Local Circuit Card AM121. When the counter is in the REMOTE mode of operation, front-panel controls and switches are inoperative except for the SAMPLE RATE control, and then only under certain programming instructions from the GPIB controller.

### 1-11. Converter A2. (Fig. 1-4.)

a. Converter A2 translates the Band B input microwave frequencies down to frequencies between 100 and 360 MHz. Translation is done by mixing the input frequencies with a reference frequency to produce, by heterodyne action, an amplified intermediate frequency. The IF is then fed to A106 through Delay Line A112 for counting and processing in Basic Counter A1.

b. Generation of the heterodyning reference frequency starts by generating a 200 MHz reference signal in Source/Amplifier A201. The 200 MHz reference in A201 is generated by an L-C oscillator phase-locked to 10 MHz from Reference Oscillator Buffer A108. The 200 MHz outputs from A201 are directed to YIG (Yttrium-Iron-Garnet) Comb Generator A207 and to Gate Generator A105 in Basic Counter A1. A power amplifier section on A201 amplifies the 200 MHz signal before it is applied to A207. The 200 MHz output to A105 is used to generate a Band B gate or may be used for a TEST 200 MHz self-test.

c. The local oscillator, or reference harmonic, frequency is generated in YIG Comb Generator A207 by taking the 200 MHz signal from A201 and converting it to a train of narrow pulses containing all harmonics of 200 MHz up to 18 GHz. This conversion is done by the YIG comb generator and a two-stage YIG filter, which selects the desired 200 MHz harmonic. The YIG filter is tuned by varying the current through a pair of coils, which change magnetic fields in the assembly.

d. Band B input signals are applied to Limiter/Attenuator A206. A passive diode limiter protects Mixer A205 from power levels in excess of one watt peak (+30 dBm). A multistage matched PIN diode attenuator section controls the RF signal level to the mixer and switches off the input signal during portions of converter operation.

e. Mixer A205 is an integrated microwave circuit assembly consisting of a hybrid coupler, termination, mixer diode, and dc return. The mixer produces two output signals on a common line: an IF signal equal to the difference frequency between the incoming RF signal from A206 and the reference frequency harmonic from A207, and a video signal resulting from rectification (detection) of either the RF or reference inputs. The mixer output is fed to I.F. Processor A204.

f. The IF and video signals from Mixer A205 are separated in A204. The IF signal is amplified by the IF amplifier and sent on as the converter IF signal to A106, through Delay Line A112, for

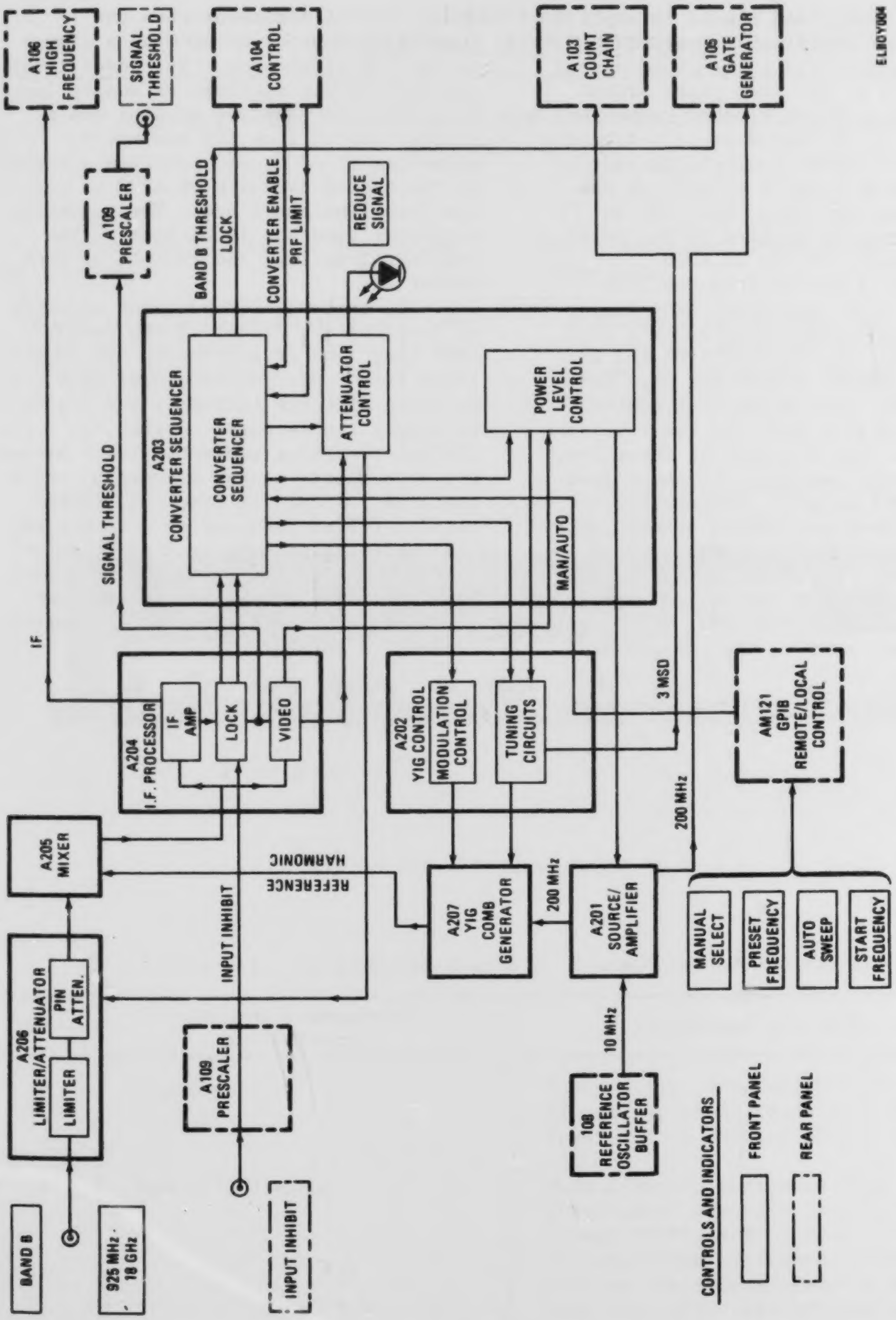

A106 HIGH FREQUENCY
SIGNAL THRESHOLD
A104 CONTROL
A103 COUNT CHAIN
A105 GATE GENERATOR
EL0OY004
A109 PRESCALER
BAND B THRESHOLD
LOCK
CONVERTER ENABLE
PRF LIMIT
REDUCE SIGNAL
SIGNAL THRESHOLD
A203 CONVERTER SEQUENCER
CONVERTER SEQUENCER
ATTENUATOR CONTROL
POWER LEVEL CONTROL
MAN/AUTO
IF
A204 I.F. PROCESSOR
IF AMP
LOCK
VIDEO
A202 YIG CONTROL
MODULATION CONTROL
TUNING CIRCUITS
3 MSD
AM121 GPIB REMOTE/LOCAL CONTROL
200 MHz
A205 MIXER
HARMONIC
REFERENCE
INPUT INHIBIT
A207 YIG COMB GENERATOR
200 MHz
A201 SOURCE/ AMPLIFIER
MANUAL SELECT
PRESET FREQUENCY
AUTO SWEEP
START FREQUENCY
A206 LIMITER/ATTENUATOR
LIMITER
PIN ATTEN.
A109 PRESCALER
10 MHz
108 REFERENCE OSCILLATOR BUFFER
CONTROLS AND INDICATORS
FRONT PANEL
REAR PANEL
BAND B
925 MHz - 18 GHz
INPUT INHIBIT

Figure 1-4. Converter A2, Functional Block Diagram

counting. The video signal is amplified in the video amplifier to produce three video outputs: (1) a threshold signal is directed to the rear-panel SIGNAL THRESHOLD connector through Prescaler A109; (2) a threshold signal, identified as attenuator control, is sent to an attenuator control circuit on Converter Sequencer A203; and (3) an analog output is applied to the power level control portion of A203.

g. On A203, inputs from the lock section of I.F. Processor A204 are sequenced and timed to produce a lock level signal for Control A104 and a Band B threshold signal for Gate Generator A105. The attenuator control threshold signal from the video section of A204 is combined with an input from the converter sequencer in the attenuator control to give two outputs: (1) an attenuator control signal, activated at a level approximately 7 dB above signal threshold, sent to the PIN attenuator of A206, to reduce signal level into Mixer A205; and (2) a reduce signal level sent to the front-panel REDUCE SIGNAL indicator when the attenuator control is sending a signal to the PIN attenuator. The power level control circuit receives an analog input from the video section of A204 and a digital signal from the converter sequencer of A203, and provides a signal to the tuning circuits of A202 to set the comb line amplitude. The converter sequencer function is to control the sensing, leveling, and control of Converter A2.

h. YIG Control A202 contains circuits to step the YIG filter to the proper comb line, and is controlled by input lines from Converter Sequencer A204. On-board circuits include a YIG driver to supply the required current, a digital-to-analog converter (DAC) to set the approximate center frequency, and a centering circuit to precisely center the YIG filter passband on a comb line. The centering process is done by modulating the YIG center frequency by an auxiliary modulation coil in YIG Comb Generator A207. The modulation control circuit is on A202.

# CHAPTER 2
# OPERATING INSTRUCTIONS

## Section I. DESCRIPTION AND USE OF OPERATOR'S CONTROLS AND INDICATORS

2-1. Front-Panel Controls, Connectors and Indicators.

Operator's front-panel controls, connectors and indicators are shown in figure 2-1 and are keyed to table 2-1, which describes their functions.

2-2. Rear-panel Controls and Connectors.

Operator's rear-panel controls and connectors are shown in figure 2-2 and are keyed to table 2-2, which describes their functions.

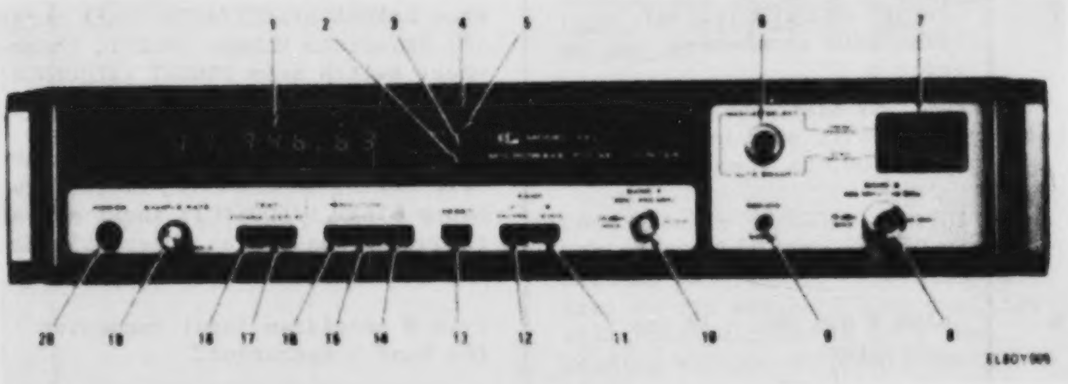


Figure 2-1. Counter Front Panel

Table 2-1. Front-panel Controls, Connectors and Indicators

| Key | Control, connector or indicator | Functional operation |
|---|---|---|
| 1 | Display | Seven-digit LED display provides direct numerical readout of input frequency in GHz and MHz. |
| 2 | REMOTE indicator | When lighted, indicates that all front-panel controls are disabled except SAMPLE RATE. This indicator is controlled by digital programmed data on the General Purpose Interface Bus (GPIB) and by rear-panel ADDRESS SWITCH. |

Table 2-1. Front-panel Controls, Connectors and Indicators - Continued

| Key | Control, connector or indicator | Functional operation |
|---|---|---|
| 3 | GATE indicator | Lights when counter is in measurement portion of cycle. |
| 4 | LEVEL indicator | Lights when input signal level is high enough to be counted. Light will blink if signal pulse repetition frequency is too low. |
| 5 | LOCK indicator | Lights when input signal has been acquired. |
| 6 | MANUAL SELECT/AUTO SWEEP switch | Selects either manual or automatic operation of counter for BAND B. |
| 7 | PRESET FREQUENCY/START FREQUENCY thumbwheel switch | When MANUAL SELECT/AUTO SWEEP switch (6) is set to MANUAL SELECT, thumbwheel switch sets PRESET FREQUENCY; input signal frequency must be 105 to 325 MHz higher. When MANUAL SELECT/AUTO SWEEP switch is set to AUTO SWEEP, thumbwheel switch sets sweep START FREQUENCY; input signal frequency must be at least 105 MHz higher than sweep start. |
| 8 | BAND B 925 MHz - 18 GHz connector | Type N precision input connector for Band B operation. |
| 9 | REDUCE SIGNAL indicator | Lights when Band B input power approaches maximum safe operating level. |
| 10 | BAND A 300 - 950 MHz connector | Type BNC input connector for Band A operation. |
| 11 | BAND B pushbutton switch | Selects Band B operation for frequencies between 925 MHz and 18 GHz. |
| 12 | BAND A pushbutton switch | Selects Band A operation for frequencies between 300 and 950 MHz. |
| 13 | RESET pushbutton switch | When pushed and released, overrides SAMPLE RATE control, resets display to zeros, and initiates a new reading. |
| 14 | 1 ms GATE pushbutton switch | When pushed in, provides 10 kHz resolution with 1 millisecond gate time on Band B or 4 millisecond gate time on Band A for reduced pulse averaging error. |

Table 2-1. Front-panel Controls, Connectors and Indicators - Continued

| Key | Control, connector or indicator | Functional operation |
|---|---|---|
| 15 | Right RESOLUTION pushbutton switch | Provides blanking of least significant digit for resolution of 100 kHz with 100 microsecond gate time on Band B or 400 microsecond gate time on Band A. |
| 16 | Left RESOLUTION pushbutton switch | Provides blanking of two least significant digits for resolution of 1 MHz with 100 microsecond gate time on Band B or 400 microsecond gate time on Band A. |
| 17 | TEST DISPLAY pushbutton switch | When pushed and held in, provides test of all segments of display LEDS. Display should read 88 888.88. |
| 18 | TEST 200 MHz pushbutton switch | When pushed and held in, provides check of counting circuits. Display should indicate 200.00 MHz. |
| 19 | SAMPLE RATE control | Continuously variable control which varies display time from 0.1 to 10 seconds per reading. Rotating control to its switched HOLD position will cause display to hold last reading without an update until RESET switch (13) is pushed in. |
| 20 | POWER pushbutton switch | When pushed in and released, power counter is turned on or off. When power is on, a green indicator is visible in switch. |

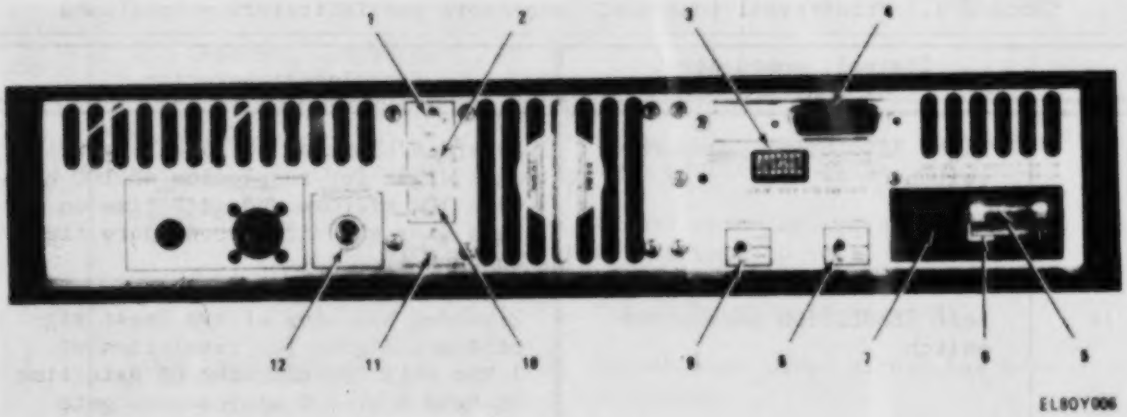


Figure 2-2. Counter Rear Panel

Table 2-2. Rear-panel Controls and Connectors

| Key | Control or connector | Functional operation |
|---|---|---|
| 1 | 10 MHz OUTPUT connector | Provides output of internal 10 MHz clock; 1 Vp-p minimum into 50 ohms. |
| 2 | SIGNAL THRESHOLD OUTPUT connector | Provides pulse output representing signal threshold level of input pulse. Output pulse typically delayed 20 nanoseconds from input pulse. Used for frequency profile measurements. |
| 3 | GPIB IEEE STD 488/1975 ADDRESS SWITCH | Address switches of counter when General Purpose Interface Bus (GPIB) is used. Setting of various combinations of seven switches permits the counter to be operated in Talk, Listen, or Monitor modes when external GPIB controller is connected to counter. |
| 4 | GPIB IEEE STD 488/1975 connector | Provides connection to external GPIB controller. |
| 5 | Fuse | Slow-blow line fuse; 1.5 A at 115 Vac or 0.75 A at 230 Vac. |
| 6 | Line voltage selector card | Selects either 115 or 230 Vac line voltage. Selected voltage printed on card is visible when card is installed. |

Table 2-2. Rear-panel Controls and Connectors - Continued

| Key | Control or connector | Functional operation |
|---|---|---|
| 7 | AC power connector | Three-prong male connector for ac power cable. Third conductor grounding meets NEC and UL requirements. |
| 8 | MIN. PRF switch | Selects minimum prf. Normally set to 50 Hz position. In 0 position, counter will measure very low prf signals but reading will not automatically reset when signal is removed. |
| 9 | STORAGE switch | Controls display update. Normally ON; in OFF position front-panel display updates continuously during measurement cycle. |
| 10 | GATE OUTPUT connector | Provides gate pulse representing actual time at which measurement is being made. Used in frequency profile measurements. |
| 11 | INPUT INHIBIT connector | Connector for external pulse input for use in frequency profile measurements. |
| 12 | ACCESSORY POWER OUT connector | Provides +5, -5.2, +12, and -12 Vdc for accessories used with counter, such as EIP Model 400 Delay Generator. |

## Section II. PREVENTIVE MAINTENANCE CHECKS AND SERVICES

### 2-3. General Instructions.

a. Before you operate. Always keep in mind the CAUTIONS and WARNINGS. Perform your before (B) PMCS.

b. While you operate. Always keep in mind the CAUTIONS and WARNINGS. Perform your during (D) PMCS.

c. After you operate. Be sure to perform your after (A) PMCS.

d. If your equipment fails to operate. Troubleshoot with proper equipment. Report any deficiencies using the proper forms. See TM 38-750.

### 2-4. PMCS Procedures.

Table 2-3 outlines the functions to be performed at specific intervals. These checks and services are to maintain Army electronic equipment in a combat serviceable condition; that is, in good general (physical) condition and in good operating condition. To assist operators in maintaining combat serviceability, the chart indicates what to check. If any entry appears in the "Equipment is not ready/available if:" column, appropriate corrective maintenance action must be taken to restore the counter to an operational condition.

## 2-5. Cleaning Instructions.

a. At the interval specified in table 2-3, remove dust and loose dirt with a clean soft cloth.

CAUTION

Do not use any solvent except water or a mild detergent to clean the plastic front panel of the counter. Other solvents may damage the panel.

b. Clean external surfaces with a clean soft cloth moistened with clean water. A mild detergent may be used for more effective cleaning.

Table 2-3. Operator Preventive Maintenance Checks and Services

NOTE

Within designated interval, these checks are to be performed in the order listed.

B - Before
D - During
A - After
W - Weekly
M - Monthly

| Item No. | Interval | | | | | Item to be inspected | Procedures - check for and have repaired or adjusted as necessary | Equipment is not ready/ available if: |
|---|---|---|---|---|---|---|---|---|
| | B | D | A | W | M | | | |
| 1 | x | | | | | Completeness | Power cable connected to counter. | Power cable is missing. |
| 2 | | x | | | | Power cable | Cuts or cracks in outside jacket; damage to connector pins. | Power cable is defective. |
| 3 | | | | x | | Controls and hardware | Missing or loose knobs or hardware | |
| 4 | | | | | x | Exterior surfaces | Clean exterior surfaces. | |
| 5 | | | | | x | Nameplate | Legibility. | |
| 6 | x | | | | | Operational capability | Perform self-test, para 2-7b(2). | Self-test indications are incorrect. |

## Section III. OPERATION UNDER USUAL CONDITIONS

### 2-6. Assembly and Preparation for Use.

a. Unpacking.

(1) Visually inspect the shipping carton for signs of damage before opening. If there is any apparent damage, request that the shipper's agent be present when the counter is unpacked. Visible and concealed damage claims against the carrier or shipper can only be filed if the agent is present or waives his rights.

(2) Open the carton, removing instrument supports and packing materials. Carefully lift out the counter. Inspect the counter for damage. Without applying power, check the mechanical operation of all controls and switches.

b. Assembly

(1) The only assembly requirements are selection of either 115 Vac or 230 Vac line voltage and connecting the power cable to the instrument.

WARNING

Be sure only the specified power cable is used. The instrument is provided with a 3-wire cable which grounds the instrument cabinet. This cable should only be inserted in a socket outlet provided with a protective ground contact. This protective action should not be negated by the use of an extension cord without a protective ground conductor.

(2) The counter is normally shipped ready for operation from a 115 Vac power line, with a 1.5 ampere slow-blow fuse installed. Check the marking on the line voltage selector card (6, fig. 2-2), visible through the window in the fuse cover, to be certain that it reads 115 volts.

CAUTION

The FUSE PULL lever attached to the body of the power module housing does not come off. Firm but careful rotation of the fuse puller will lift up one end of the fuse so that finger force can remove the fuse. Failure to heed this caution by exerting too much force may damage the plastic pivot of the built-in fuse puller.

(3) Remove the installed fuse by lifting up on the FUSE PULL lever and check that it is a 1.5 ampere fuse.

(4) Reinstall or replace the fuse with one of the correct value and connect the power cable to the ac power connector.

(5) To change the line voltage operation, proceed as follows:

(a) On the rear of the counter, slide the fuse cover to the left and remove the fuse by lifting up on the FUSE PULL lever; see CAUTION above.

(b) Extract the line voltage selector card.

(c) Rotate the card so that the appropriate marking (115 or 230 volts) will be visible when the card is inserted into the card slot. Carefully but firmly insert the card into the slot, being careful not to cant or tilt the card while inserting. Check the seating by sliding the fuse cover from left to right. After checking the card seating, slide the fuse cover back to the left to gain access to the fuse clip.

(d) Insert a slow-blow fuse of the correct value (1.5 amperes for 115 Vac, 0.75 ampere for 230 Vac) in the fuse clip; check that built-in fuse puller does not obstruct the fuse cover by sliding the fuse cover to the right.

(e) Connect the power cable to the ac power connector.

c. Preparation for Use.

(1) Stand-alone Operation. No special procedures are necessary if the counter is used as a stand-alone test instrument. Applying power and connecting the signal to the selected connector and selecting the desired switches and controls is all that is required.

(2) GPIB Operation. Installation of the counter in a GPIB-controlled system will vary with console or rack hardware. Therefore only general procedures can be suggested.

(a) The dimensions of the counter are 3.5 inches high by 16.75 inches wide by 19 inches deep. Rack mounting kits are available from the manufacturer of the counter to mount the instrument in a standard 19 inch width rack-mount cabinet or console. Ventilation of the counter is through the rear panel so it is not necessary or desirable to remove the top and bottom covers for cooling. Top and bottom covers should remain in place secured by screws to retain RFI integrity.

(b) Access to the rear panel is required to control selector switches and the GPIB address switches. The rear panel ventilating louvers and blower should not be blocked off from free air flow.

(c) Leads from frequency sources to the counter front-panel connectors should be as short as possible. A common ground bus should tie the counter to other instruments and the GPIB controller. The length of power cable is not critical but the supplied cable should be retained and plugged into a powerline strip.

(d) The length of the GPIB interface cable should be as short as feasible and should be shielded against RFI to reduce data transmission contamination. Any keyboarding or fixed program controller may be connected, provided that the controller meets IEEE Standard 488/1975.

## 2-7. Operation as Stand-alone Instrument.

a. Operating Modes. The counter has three principal modes of operation: automatic, manual, and externally enabled. Operation on Band A (300 - 950 MHz) is automatic; operation on Band B (925 MHz - 18 GHz) may be either automatic or manual. Externally enabled operation covers specific measurement techniques. Signals may be connected to both the BAND A and BAND B inputs at the same time, but the counter will display only the input frequency selected by the appropriate BAND pushbutton switch on the front panel.

b. Preliminary Procedures.

(1) Rear-panel Switches. Set rear-panel switches as follows.

(a) GPIB IEEE STD 488/1975 ADDRESS SWITCH 7 to 0 (top of switch depressed).

(b) MIN. PRF switch to 50 Hz.

(c) STORAGE switch to ON.

(2) Self-test.

(a) Press the POWER switch to turn on the counter. The display should light and the internal cooling fan should operate.

(b) Partially depress either of the two RESOLUTION switches and release it, so that neither switch remains in a depressed position. All digits in the display should indicate zero.

(c) Press the TEST DISPLAY switch. The display should indicate 88 888,88 while the switch is held in. Release the switch.

(d) Press the TEST 200 MHz switch. The display should indicate 200.00, with the two leading zeros blanked (unlighted), while the switch is held in. Release the switch.

(e) Press the right RESOLUTION switch and again hold the TEST 200 MHz switch in. The display should indicate 200.0, with the two leading zeros blanked. Release the switch.

(f) Press each RESOLUTION switch in turn and note that the display digit immediately above the switch which has been depressed, and any digit to the right, is blanked.

(g) Unblank all display digits by repeating step (b).

c. Band A (300 - 950 MHz) Operation.

### CAUTION

Peak power applied to the BAND A input connector should be between -10 and +10 dBm for normal operation. Peak input must not exceed +27 dBm or damage to the counter may result, even if the counter is turned off.

(1) Perform the preliminary procedures of step b., above.
(2) Connect the signal source to the BAND A input connector.
(3) Depress the BAND A switch.
(4) Depress the desired RESOLUTION switch.
(5) If the input signal level is high enough for counting, both the LEVEL and LOCK indicators will light, and the measured frequency will be displayed.

NOTE

The REDUCE SIGNAL indicator is inoperative on Band A.

(6) Turn the SAMPLE RATE control to provide the desired display update rate. The GATE indicator will flash in accordance with the sample rate. If the control is set to its switched HOLD position, the display will retain the last reading. If a new reading is desired, press and release the RESET switch.

d. Band B (925 MHz - 18 GHz) Operation.

CAUTION

Peak power applied to the BAND B input connector should be within the following ranges for normal operation:

925 MHz - 10 GHz: -10 to +10 dBm

10 - 18 GHz: -5 to +10 dBm.

The peak input power must not exceed +30 dBm or damage to the counter may result, even if the counter is turned off.

(1) Initial Procedures.
(a) Perform the preliminary procedures of step b above.
(b) Connect the signal source to the BAND B input connector.
(c) Depress the BAND B switch.
(d) Depress the desired RESOLUTION switch.
(e) If the input signal level is high enough for counting, both the LEVEL and LOCK indicators will light. If the REDUCE SIGNAL indicator lights, the input signal power is approaching the maximum safe operating level and should be reduced.

(2) Automatic Mode. In the automatic mode, the counter searches for the input signal by sweeping from a start frequency which is 105 MHz above a preset frequency.
(a) Set the MANUAL SELECT/AUTO SWEEP switch to AUTO SWEEP. For full search, set the START SWEEP thumbwheel switches to 00.0 GHz.
(b) To improve acquisition speed, the sweep start frequency may be set by means of the START SWEEP thumbwheel switches. The lowest frequency which can then be acquired and displayed will be 105 MHz above the switch settings; erroneous readings may be displayed if the frequency of the applied signal is less than 105 MHz above the switch settings.
(c) Adjust the SAMPLE RATE control as described in paragraph 2-7c(6).

(3) Manual Mode. In the manual mode, the search sweep is inhibited, reducing the acquisition time. However, the signal frequency to be measured must be between 105 and 325 MHz above a preset frequency.
(a) Set the MANUAL SELECT/AUTO SWEEP switch to MANUAL SELECT.
(b) Set the PRESET FREQUENCY thumbwheel switches so that they indicate a frequency 105 to 325 MHz lower than the signal frequency. For example, if the frequency to be measured is expected to be 12.35 GHz, the thumbwheel switches should be set to indicate 12.2 GHz, which places the input frequency 105 to 325 MHz above the preset frequency. Erroneous readings may be displayed if the frequency of the applied signal is outside the preset range.
(c) Adjust the SAMPLE RATE control as described in paragraph 2-7c(6).

### 2-8. Externally Enabled Operation.

a. Function. The use of the rear-panel INPUT INHIBIT connector makes possible a class of measurements known as dynamic frequency measurements - measurements made at a specified point in time on a signal whose frequency is some repetitive function of time. When a high emitter-coupled-logic (ECL) level is applied, the counter is inhibited from making a measurement. Thus a signal at the INPUT INHIBIT connector can be used as an enable signal to make a measurement at a desired time. The width of the enable signal determines the duration of the measurement, typically 30 nanoseconds less than the applied pulse.

b. INPUT INHIBIT Requirements. The INPUT INHIBIT circuit is designed to be compatible with either a 50 ohm impedance pulse generator or ECL devices. An internal termination of 50 ohms returned to -2 volts makes this dual compatibility possible. An ECL high level signal (-0.8 to -1.1 V) will inhibit measurement, while an ECL low level signal (-1.5 to -2.0 V) will enable measurement. ECL devices are designed to drive 50 ohm lines without reflections when the lines are terminated with 50 ohms returned to -2 V. The direct compatibility with a 50 ohm pulse generator results from the fact that zero volts from a 50 ohm source will produce -1 V at the INPUT INHIBIT (inhibiting the counter), while a -1 V signal into 50 ohms will produce -1.5 V at the INPUT INHIBIT thus enabling the counter.

### 2-9. Pulse Profile Measurements

a. Purpose. Automatic pulse measurements can determine the average frequency of a pulse. In some cases, however, additional information may be necessary. For example, a pulse magnetron may exhibit substantial frequency shift near the leading and trailing edges of the pulse, or a pulsed Gunn diode oscillator may exhibit frequency shift during a pulse due to peak power thermal effects.

b. Measurement Technique. Measurements of these characteristics are easily made with the counter and a delaying pulse generator (see fig. 2-3).

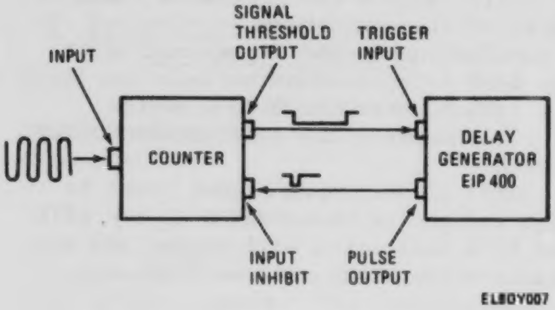


Figure 2-3. Pulse Profile Measurement Test Setup

The SIGNAL THRESHOLD OUTPUT of the counter is used to trigger the pulse generator. The generator's output pulse is used as an enable input to the counter. As the pulse delay is varied, the measurement window can be "walked" through the pulse. A plot of frequency versus delay gives the frequency-versus-time profile of the pulse directly as shown in fig. 2-4. The width of the measurement window is determined by the width of the pulse generator output. Measurement windows of 50 nanoseconds or less can be used, although wider windows yield higher accuracy.

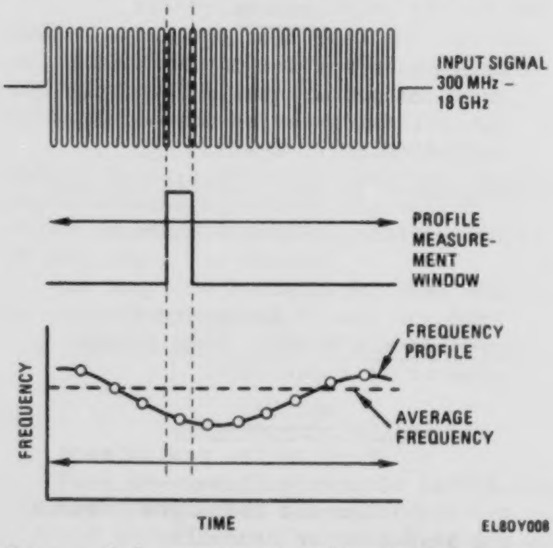


Figure 2-4. Pulse Profile Measurement

### 2-10. Dynamic Characteristics of Time Varying Signals.

a. Purpose. Many complex signals are not pulses at all but simply continuous signals whose frequency varies repetitively with time. One example is the measurement of the response of a device such as a voltage-controlled oscillator (VCO). A square wave applied to the tuning voltage will produce a response curve of frequency versus time, allowing measurement of various settling times such as post-tuning drift. Another possible application would be the measurement of linearity and amplitude for frequency-modulated radar altimeter signals.

b. Measurement Technique. Fig. 2-5 shows a test setup designed to make measurements on time varying signals. It is similar to the pulse profile test setup, except that in this case, since there is always a signal present, a trigger must be obtained from the modulating source. This will trigger the pulse generator which controls the measurement.

### 2-11. Multiple Pulse Signal Measurements.

a. Purpose. Another type of measurement is that of a repetitive sequence of pulses differing in frequency. In this case, it is desirable to measure the frequency of each pulse in the sequence separately.

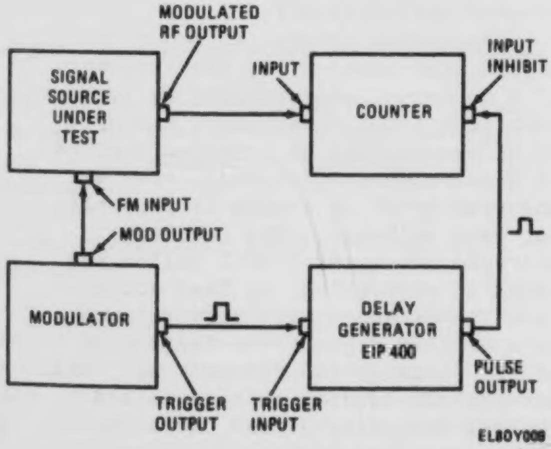


Figure 2-5. Time Varying Signal Measurement Test Setup

b. Measurement Technique. The same test setup as shown in fig. 2-5 is required, with the trigger pulse synchronous with the sequence. In this measurement, the INPUT INHIBIT is used simply to discriminate between pulses. The enabling pulse can be slightly wider than the pulse to be measured. The counter will automatically restrict the measurement window entirely within the pulse. By shifting the delay time of the enabling pulse, each input pulse of the sequence can be separately measured.

### 2-12. Timing Considerations.

a. General. Under most circumstances, internal timing within the counter is of no concern to the user. However, in applications where a few nanoseconds are significant, some details of internal operation are important. These involve two areas: measurement window width and internal timing delays.

b. Measurement Window Width. The measurement window is the period during which the gate is actually open to enable the counting of a signal. This gate width will typically be 30 nanoseconds narrower than the pulse applied to the INPUT INHIBIT connector. The width of the gate is always an integral number of clock periods (5 nanoseconds). For applications where the measurement window needs to be known to an accuracy better than 20 nanoseconds, it is recommended that the GATE OUTPUT on the rear panel be observed directly on a high speed oscilloscope. The desired gate width may then be set by varying the INPUT INHIBIT pulse width. For accurate pulse representation, the oscilloscope input should be terminated in a 50 ohm load.

c. Internal Timing Delays. When it is necessary to measure the signal frequency at a precise point in time, the internal delays of the measuring instrument can be significant. The total delay between the time a signal is applied to the counter input connector, and the time it is available to be counted, is nominally 60 nanoseconds. The SIGNAL THRESHOLD OUTPUT on the rear panel typically occurs 20 nanoseconds after the signal is applied. The GATE OUTPUT at the rear panel occurs at the measurement time with virtually no delay. In other words, when absolute time positioning of a signal is required, it is necessary to consider that the GATE OUTPUT signal, which represents the measurement period, is actually making a measurement of the signal which appeared at the input connector 60 nanoseconds earlier. If the SIGNAL THRESHOLD OUTPUT is used as an indication of input signal, then it occurs 40 nanoseconds prior to measurement. Fig. 2-6 shows the relative timing of these signals for a pulsed input signal. Timing, however, is not a function of input signal characteristics.

## 2-13. Accuracy.

### a. General Considerations.

(1) In a cw frequency counter, measurement accuracy is generally specified as time base accuracy ±1 count. This means that the frequency measurement is in error by the same percentage as the time base reference oscillator. The maximum error in the time base is the sum of various possible errors, such as aging rate, temperature, etc.

(2) The second type of error, ±1 count, is derived from the relative timing of gate and signal. Simply stated, if an event occurs every 400 milliseconds, a counter could measure either 2 or 3 events in a one second interval, since the processed input signal and the gate are asynchronous.

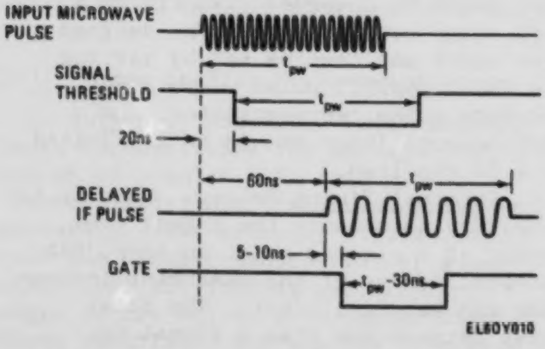


Figure 2-6. Internal Timing Delays

(3) A third possible source of error in a cw counter is gate error. A gate is supposed to represent a precise number of reference oscillator cycles. Due primarily to differences in the rise and fall times of various circuits, the actual gate will usually be a fixed amount wider or narrower than desired. If this error is less than one period of the maximum input frequency, no counter error will occur. Thus a 300 MHz counter needs a gate accurate to about 3 nanoseconds.

(4) Each of these three sources of error can contribute to the overall error in pulse frequency measurements. In fact for narrow pulses, the second and third sources of error, which are usually ignored in a cw counter, become the dominate sources of error in a pulse counter.

b. Time Base Errors. A frequency error in the time base reference oscillator results in a proportional frequency measurement error. Two main sources of time base error are aging rate and temperature. The temperature compensated crystal oscillator (TCXO) reduces temperature instability to less than 2 x $10^{-6}$. By calibration against a frequency standard, this error can be made less than one count, and thus becomes insignificant.

c. Averaging Error. In order to obtain high resolution, the frequency of a number of measurements is averaged. Each individual measurement has a ±1 count uncertainty as previously noted. If N measurements are made, then an uncertainty of ±N counts is possible, but very unlikely. The resultant averaged measurement will follow the rules of statistics, in that successive measurements will vary randomly to a certain degree. In fact, most of the readings (63 percent) will fall between $\pm\sqrt{N}$ counts; this is called the rms averaging error. N is the number of gates required to accumulate 100 microseconds or 1 millisecond of gate time. The gate is typically

30 nanoseconds narrower than the input pulse, so that

$$\text{Averaging Error (rms)} = \frac{F}{\sqrt{PW - 0.03}}$$

where PW = pulse width in microseconds

F = 200 kHz with 100 μsec gate, Band A; or 60 kHz with 1 msec gate, Band A; or 100 kHz with 100 μsec gate, Band B; or 30 kHz with 1 msec gate, Band B.

d. Gate Error.

(1) When narrow pulses are counted, the gate is opened many times in order to obtain a high resolution measurement. Each time the gate opens and closes, there will be a small but finite error. The total error is proportional to the number of times the gate is cycled during a measurement, and is thus inversely proportional to the gate width. This error is also related to both temperature and input frequency. The worst case error, including all variables, is specified for the counter as:

$$\frac{\pm 100\text{ kHz}}{PW - 0.03} \quad \text{for Band A, and}$$

$$\frac{\pm 40\text{ kHz}}{PW - 0.03} \quad \text{for Band B}$$

where PW = pulse width in microseconds.

(2) Unlike averaging error, which is random, gate error is systematic, and is not reduced by frequency averaging.

## 2-14. Techniques for Improving Accuracy.

a. Time Base Calibration. A frequency error in the time base oscillator results in the same percentage error in the frequency reading for either cw or pulsed signals. By directly measuring the 10 MHz time base frequency at the 10 MHz OUTPUT connector with a standard of known accuracy, this error can be determined and corrected. As an example, the measured time base output is 10.0001 MHz. The time base is thus $1 \times 10^{-6}$ high in frequency, and all readings will be $1 \times 10^{-6}$ low in frequency. Thus, a reading at 10 GHz will be 10 kHz low. Although the reading can be corrected for this error, the counter should be recalibrated as soon as possible.

b. Gate Error.

(1) Gate error at any given frequency and pulse width can be virtually eliminated. This is accomplished by simulating a pulse input and determining the gate error. This calibration factor can then be added to, or subtracted from, the indicated measurement to obtain the correct frequency.

(2) First, determine the gate error using a cw source at approximately the same frequency (within 25 MHz) as the indicated measurement. A pulsed input is then simulated by applying an enable signal, of the same width as the pulse to be measured, to the INPUT INHIBIT connector. Gate error is the difference in reading between the pulsed and non-pulsed measurement of the same cw signal. This procedure provides the true gate error, and avoids error associated with any possible pulling of the signal source.

## 2-15. Operation Using General Purpose Interface Bus.

a. General.

(1) The counter may be operated via the General Purpose Interface Bus (GPIB) and may be controlled by, listened to and talked to by any device or devices compatible with IEEE STD-488. Table 2-4 lists the Capability Identification Codes assigned to the counter. This code is also printed on the counter rear panel adjacent to the GPIB 24-pin connector so that programming instructions or keyboarding of a controller can be interfaced with the counter configuration and capabilities.

(2) The IEEE STD-488 GPIB system (fig. 2-7) consists of 16 signal lines

Table 2-4. Counter GPIB Capability Identification Codes

<table>
<tr><th>Identi-fication</th><th colspan="4">Description</th><th>States omitted</th><th>Other requirements</th><th>Other function subsets required</th></tr>
<tr><td>SH1</td><td colspan="4">Complete capability</td><td>None</td><td>None</td><td>T1-T8</td></tr>
<tr><td>AH1</td><td colspan="4">Complete capability</td><td>None</td><td>None</td><td>None</td></tr>
<tr><td rowspan="3">T1</td><td colspan="4">Capabilities</td><td rowspan="3">None</td><td rowspan="3">Omit (MLA ∧ ACDS)</td><td rowspan="3">SH1 and AH1</td></tr>
<tr><td>Basic Talker</td><td>Serial Poll</td><td>Talk Only Mode</td><td>Unaddress If MLA</td></tr>
<tr><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td></tr>
<tr><td rowspan="3">L4</td><td colspan="4">Capabilities</td><td rowspan="3">None</td><td rowspan="3">Include (MTA ∧ ACDS)</td><td rowspan="3">AH1 and T1-T8</td></tr>
<tr><td>Basic Listener</td><td colspan="2">Listen Only Mode</td><td>Unaddress If MTA</td></tr>
<tr><td>Yes</td><td colspan="2">No</td><td>Yes</td></tr>
<tr><td>SR1</td><td colspan="4">Complete capability</td><td>None</td><td>None</td><td>T1, T2, T5, or T6</td></tr>
<tr><td>RL2</td><td colspan="4">No local lock out</td><td>LWLS and RWLS</td><td>rtl always false</td><td>L1-L4</td></tr>
<tr><td>DC1</td><td colspan="4">Complete capability</td><td>None</td><td>None</td><td>L1-L4</td></tr>
</table>

SH = Source Handshake, AH = Acceptor Handshake, T = Talker, MLA = My Listen Address, ACDS = Accept Data State, ∧ = AND, MTA = My Talk Address, L = Listener, RL = Remote Local, DC = Device Clear, LWLS = Local With Lockout State, RWLS = Remote With Lockout State, SR = Service Request

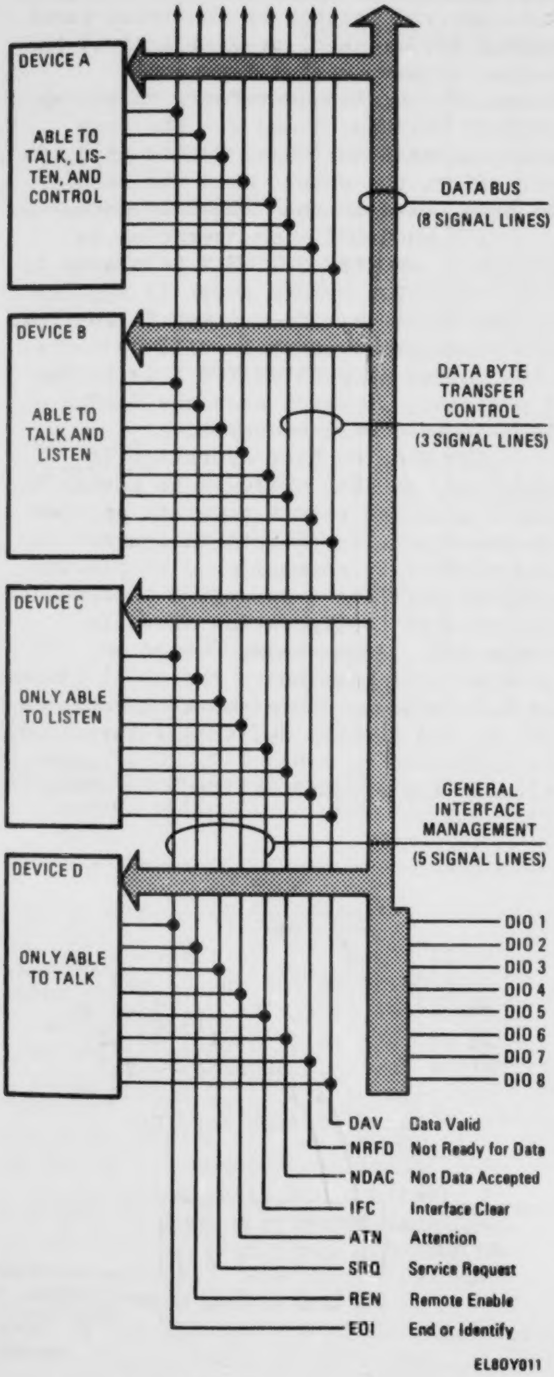

DEVICE A
ABLE TO TALK, LISTEN, AND CONTROL
DEVICE B
ABLE TO TALK AND LISTEN
DEVICE C
ONLY ABLE TO LISTEN
DEVICE D
ONLY ABLE TO TALK
DATA BUS
(8 SIGNAL LINES)
DATA BYTE TRANSFER CONTROL
(3 SIGNAL LINES)
GENERAL INTERFACE MANAGEMENT
(5 SIGNAL LINES)
DIO 1
DIO 2
DIO 3
DIO 4
DIO 5
DIO 6
DIO 7
DIO 8
DAV Data Valid
NRFD Not Ready for Data
NDAC Not Data Accepted
IFC Interface Clear
ATN Attention
SRQ Service Request
REN Remote Enable
EOI End or Identify
EL80Y011

Figure 2-7. GPIB Capabilities and Structure

used to carry data, control, and management information. The 16 lines are organized into three sets, as follows:

(a) Data Bus - 8 signal lines

(b) Data Byte Transfer Control - 3 signal lines

(c) General Interface Management - 5 signal lines.

(3) The counter is a type B device able to talk and listen (T1 and L4 codes). Mnemonics assigned to the various signal lines are as follows:

(a) Data Bus lines are:

DIO 1 through DIO 8 (Data Input/Output line 1 through 8) - used to transmit message bytes in bit-parallel, byte-serial format, asynchronously and usually in a bi-directional manner.

(b) Data Byte Transfer Control lines are:

DAV (Data Valid) - used to indicate the condition (availability and validity) of information on DIO signal lines.

NFRD (Not Ready For Data) - used to indicate the condition of readiness of device(s) to accept data.

NDAC (Not Data Accepted) - used to indicate the condition of acceptance of data by device(s).

(c) General Interface Management lines are:

ATN (Attention) - used by a controller to specify how data on the DIO signal lines are to be interpreted and which devices must respond to the data.

IFC (Interface Clear) - used by a controller to place the interface system, portions of which are contained in all interconnected devices, in a known quiescent state.

SRQ (Service Request) - used by a device to indicate the need for attention and to request an interruption of the current sequence of events.

REN (Remote Enable) - used by a controller (in conjunction with other messages) to select between two alternate sources of device programming data.

EOI (End Or Identify) - used by a talker to indicate the end of a multiple byte transfer sequence or, in conjunction with ATN (by a controller), to execute a polling sequence.

NOTE

The EOI function is not included in this counter.

(4) The 16 GPIB lines are connected to the rear-panel GPIB IEEE STD 488/1975 connector as shown in table 2-5. To the left of and below the connector are seven ADDRESS SWITCHes for setting the GPIB modes or addresses of the counter.

b. On Line and Off Line Operation.

(1) The Talk Only On Line and Off Line operation are summarized in table 2-6. The setting of ADDRESS SWITCH 7 determines the mode of operation of the counter. When the switch is set to the 1 position before power is applied to the counter, the counter can be a talker only with continuous output from the GPIB connector. Selection of sample rate control (either by the front-panel SAMPLE RATE control or Fast Active) and output format (either Exponent-Scientific or Exponent-Four) is set by ADDRESS SWITCHes 1 and 2. The four other ADDRESS SWITCHes, 3 through 6, do not effect the output when the counter is being used in the Talk Only mode.

Table 2-5. GPIB IEEE STD 488/1975 Connector Pin Assignments

| Pin | Signal line | Pin | Signal line |
|---|---|---|---|
| 1 | DIO 1 | 13 | DIO 5 |
| 2 | DIO 2 | 14 | DIO 6 |
| 3 | DIO 3 | 15 | DIO 7 |
| 4 | DIO 4 | 16 | DIO 8 |
| 5 | EOI | 17 | REN |
|  | (not used) | 18 | Gnd (6)* |
| 6 | DAV | 19 | Gnd (7)* |
| 7 | NRFD | 20 | Gnd (8)* |
| 8 | NDAC | 21 | Gnd (9)* |
| 9 | IFC | 22 | Gnd (10)* |
| 10 | SRQ | 23 | Gnd (11)* |
| 11 | ATN | 24 | Gnd (Logic)* |
| 12 | (Shield) |  |  |

*Gnd ( ) refers to the signal ground return of the referenced contact pin; EOI and REN (5, 17) ground return on pin 24.

(2) When Off Line operation is selected, ADDRESS SWITCH 7 is placed in the 1 position before power is applied to the counter. After power is applied, the front-panel controls will be operative unless ADDRESS SWITCH 1 is in the 1 position, in which case the SAMPLE RATE control will be inactive.

(3) When On Line operation is selected, ADDRESS SWITCH 7 is placed in the 0 position before power is applied to the counter. Address assignment to the counter is accomplished by placing ADDRESS SWITCHes 1 through 5 in the appropriate configuration shown in table 2-6. After being turned on, the counter will respond to the ASCII Listen or Talk Address character that has been set by the ADDRESS SWITCHes 1 through 5, as indicated in table 2-7. Configuration of the ADDRESS SWITCHes is shown in fig. 2-8.

NOTE

ASCII ? and _____ is reserved for GPIB Unlisten and Untalk and therefore cannot be assigned as an address to a counter or any other device. ADDRESS SWITCH settings of 1 1 1 1 0 cannot be used as an address for the counter.

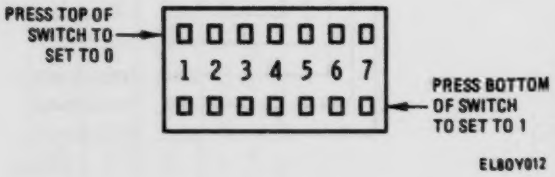

PRESS TOP OF SWITCH TO SET TO 0
1 2 3 4 5 6 7
PRESS BOTTOM OF SWITCH TO SET TO 1
EL80V012

Figure 2-8. GPIB IEEE STD 488/1975 ADDRESS SWITCH Positions

Table 2-6. On Line and Off Line ADDRESS SWITCH Settings

| Mode | ADDRESS SWITCH | | | | | | | Function |
|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | |
| On Line Operation | A1 | A2 | A3 | A4 | A5 | x | 0 | Address assignment to counter. ADDRESS SWITCH 7 must be in 0 position. |
| Off Line Operation | 0* | 0* | x | x | x | x | 1 | Continuous output determined by SAMPLE RATE control. Exponent in scientific format. |
| | 1* | 0* | x | x | x | x | 1 | Continuous output, fast active. SAMPLE RATE control inactive. Exponent in scientific format. |
| | 0* | 1* | x | x | x | x | 1 | Continuous output determined by SAMPLE RATE control. Exponent-four output format. |
| | 1* | 1* | x | x | x | x | 1 | Continuous output, fast active. SAMPLE RATE control inactive. Exponent-four output format. |
| | x* | x* | x | x | x | x | 0 | No output |

x = Don't care

* = May be continuously set or reset as long as ADDRESS SWITCH 7 is set to 1 during power application. After application of power, ADDRESS SWITCH 7 may be set to 0.

c. Remote/Local Operation.

(1) In addition to On Line and Off Line modes of operation, the GPIB provides for Remote and Local Operation. In Remote Operation, the counter is On Line and is under control of programming signals from a controller. In Local Operation, the counter front-panel controls are active and controller signals do not affect counter operation; however, output signals are available to the GPIB (Talker Only Mode) depending on the counter rear-panel ADDRESS SWITCH settings. The controller can switch between Remote and Local by sending the appropriate ASCII codes for Remote Enable (REN) or Go To Local control (GTL) to the counter.

(2) When the counter is On Line and in Remote and the controller has selected the counter with ATN (Attention) to the counter address followed by Listen, the counter will respond to programming instructions from the controller. Programming instructions can select all control functions of the counter front panel except power on/off, sample rate, and self-test. Programming instructions from the controller to the counter are identified as Device Dependent Data.

d. Device Independent Data, On Line Operation. Device independent data consists of the following, which are sent by controller while in the command mode.

(1) Go To Local (GTL). An addressed command given by the controller. The counter must have received its Listen address prior to the GTL

Table 2-7. ADDRESS SWITCH Settings vs ASCII Characters

| ADDRESS SWITCH | | | | | ASCII Listen address character | ASCII Talk address character | *Decimal Talk/Listen address |
|---|---|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | 5 | | | |
| Setting | | | | | | | |
| 0 | 0 | 0 | 0 | 1 | SP | @ | 00 |
| 1 | 0 | 0 | 0 | 1 | ! | A | 01 |
| 0 | 1 | 0 | 0 | 1 | " | B | 02 |
| 1 | 1 | 0 | 0 | 1 | # | C | 03 |
| 0 | 0 | 1 | 0 | 1 | $ | D | 04 |
| 1 | 0 | 1 | 0 | 1 | % | E | 05 |
| 0 | 1 | 1 | 0 | 1 | & | F | 06 |
| 1 | 1 | 1 | 0 | 1 | ' | G | 07 |
| 0 | 0 | 0 | 1 | 1 | ( | H | 08 |
| 1 | 0 | 0 | 1 | 1 | ) | I | 09 |
| 0 | 1 | 0 | 1 | 1 | * | J | 10 |
| 1 | 1 | 0 | 1 | 1 | + | K | 11 |
| 0 | 0 | 1 | 1 | 1 | , | L | 12 |
| 1 | 0 | 1 | 1 | 1 | – | M | 13 |
| 0 | 1 | 1 | 1 | 1 | . | N | 14 |
| 1 | 1 | 1 | 1 | 1 | / | O | 15 |
| 0 | 0 | 0 | 0 | 0 | 0 | P | 16 |
| 1 | 0 | 0 | 0 | 0 | 1 | Q | 17 |
| 0 | 1 | 0 | 0 | 0 | 2 | R | 18 |
| 1 | 1 | 0 | 0 | 0 | 3 | S | 19 |
| 0 | 0 | 1 | 0 | 0 | 4 | T | 20 |
| 1 | 0 | 1 | 0 | 0 | 5 | U | 21 |
| 0 | 1 | 1 | 0 | 0 | 6 | V | 22 |
| 1 | 1 | 1 | 0 | 0 | 7 | W | 23 |
| 0 | 0 | 0 | 1 | 0 | 8 | X | 24 |
| 1 | 0 | 0 | 1 | 0 | 9 | Y | 25 |
| 0 | 1 | 0 | 1 | 0 | : | Z | 26 |
| 1 | 1 | 0 | 1 | 0 | ; | [ | 27 |
| 0 | 0 | 1 | 1 | 0 | < | \ | 28 |
| 1 | 0 | 1 | 1 | 0 | = | ] | 29 |
| 0 | 1 | 1 | 1 | 0 | > | ⌢ | 30 |

*Decimal Talk/Listen addresses are provided as a cross-reference for controllers which use them in their program instructions.

command being issued. When GTL is received, the counter will go to the Local mode with all front-panel switches operative. Fast Cycle, or the last YIG Preset command received by the counter while in the Remote mode, will remain and will not be cleared by this command. The front-panel REMOTE indicator will be off.

(2) Selected Device Clear (SDC). An addressed command given by the controller. The counter must have received its Listen address prior to the SDC command being issued. When SDC is received, the counter will be cleared to its initial state and remains addressed to Talk or Listen. ADDRESS SWITCHes 1 - 7 will be read.

(3) Device Clear (DCL). Same as SDC command, except that counter's Listen address does not have to be received prior to issuing of DCL.

(4) Serial Poll Enable (SPE). An addressed command given by the controller.

(5) Serial Poll Disable (SPD). An addressed command which negates SPE.

e. Device Dependent Data, On Line Operation.

(1) Definition. Device dependent data is that data, inputted in string form, to which the counter uniquely responds while in the Remote mode, and while addressed to Listen.

(2) Implementation. While in the command mode, the controller places the counter in the Remote mode by setting the REN line active, then by sending the listen address of the counter. When the counter is in the Remote mode and addressed to Listen, the controller leaves the command mode and enters the data transfer mode. It is in this mode and counter setup that device dependent data can be sent by the programmer. The mnemonics, format, and specifications for the device dependent data are described below and summarized in table 2-8.

(3) Format. The format for device dependent data from a controller is as follows:

Mnemonic Sign Value Scale Factor

(a) Mnemonic. Two alpha, or one alpha and one numeric, characters, depending on the function being programmed.

(b) Sign. The sign "+" or "-" of the value portion of the function being programmed. (The "+" sign is optional.)

(c) Value. The particular numeric value assigned to the function being programmed. Leading and trailing zeros need not be programmed.

(d) Scale Factor. Exponent symbol used with the value portion of the function being programmed M = megahertz ($10^6$), G = gigahertz ($10^9$).

NOTE

> If any of the above does not pertain to the particular function being programmed, it should be omitted.
>
> For example, BA: BA is the Mnemonic. The Sign, Value, and Scale Factor are not necessary. This function sets the counter to Band A.

(4) Mnemonics.

(a) YIG Preset (YP). This command will program a YIG Preset equal to the Value and Scale Factor. Negative YIG Presets will be taken as positive. Mnemonic YP, Sign + (optional), Value and Scale Factor.

Example: YP 1.2 G or YP - 1.2 G. Both program 1.2 x $10^9$ Hz (1.2 GHz) into the counter.

Example: YP M or YP G: Clears the YIG Preset.

Between YP and M or G, only the Sign, numeric Value, or decimal point will be recognized by the counter. YIG preset information will be updated only during a converter reset.

NOTE

> In the following commands, the Mnemonic is shown following the command title. Sign, Value, and Scale Factor are not used.

Table 2-8. Programming Summary

| Function | ASCII | Mnemonic | Sign | Value | Scale Factor | Comments |
|---|---|---|---|---|---|---|
| YIG Preset |  | YP | + | YIG preset range | M or G | + sign optional |
| Cycle Counter |  | CC |  |  |  | One-shot action |
| Reset Counter and Converter |  | RC |  |  |  | One-shot action |
| Converter Auto |  | CA |  |  |  |  |
| Converter Manual |  | CM |  |  |  |  |
| Hold Active |  | HA |  |  |  | No data transmission |
| Hold Passive |  | HP |  |  |  |  |
| 1 ms Gate Time Active |  | TA |  |  |  | Gate time: 1 ms |
| 1 ms Gate Time Passive |  | TP |  |  |  | Gate time: 100 µs |
| Band A |  | BA |  |  |  |  |
| Band B |  | BB |  |  |  |  |
| Remote Resolution: 10 kHz |  | R4 |  |  |  |  |
| Remote Resolution: 100 kHz |  | R5 |  |  |  |  |
| Remote Resolution: 1 MHz |  | R6 |  |  |  |  |
| Fast Active |  | FA |  |  |  | Sample rate |
| Fast Passive |  | FP |  |  |  | Sample rate |
| Transmit Normal |  | TN |  |  |  |  |
| Transmit Service Request |  | TS |  |  |  |  |
| Exponent-Scientific |  | ES |  |  |  | Output data |
| Exponent-Four |  | E4 |  |  |  | Output data |

Table 2-8. Programming Summary - Continued

| Function | ASCII | Mnemonic | Sign | Value | Scale Factor | Comments |
|---|---|---|---|---|---|---|
| Device Clear (DCL) | DC4 | | | | | Controller dependent |
| Selected Device Clear (SDC) | EOT | | | | | Controller dependent |
| Go to Local Control (GTL) | SOH | | | | | Controller dependent |
| Serial Poll Enable (SPE) | CAN | | | | | Controller dependent |
| Serial Poll Disable (SPD) | EM | | | | | Controller dependent |
| My Listen Address (MLA) | | | | | | Device dependent |
| My Talk Address (MTA) | | | | | | Device dependent |
| Unlisten | ? | | | | | Controller dependent |
| Untalk | — | | | | | Controller dependent |

(b) Cycle Counter (CC). This command resets the basic counter section, and causes it to take a new reading. When the CC command is sent, reset occurs; to obtain another reset, CC must be resent.

(c) Reset Counter and Converter (RC). This command resets both the basic counter and converter sections, and causes the counter to take a new reading. When RC is sent, a reset occurs; to obtain another reset, RC must be sent again.

(d) Hold Active (HA). When HA is sent in the Remote mode, the counter stops taking readings, data transmission is stopped, and the last frequency read is displayed and held by the counter. In the Fast Active mode (subparagraph (s) below), the HA command will have no effect upon the counter's display operation while in the Local mode, but will stop data transmission. If programmed during the FA mode, and FA is then terminated, the counter will respond to the HA command.

(e) Hold Passive (HP). This command terminates HA.

(f) 1 ms Gate Time Active (TA). This command puts the counter in the 1 ms gate time mode.

(g) 1 ms Gate Time Passive (TP). This command terminates TA.

(h) Band A (BA). This command selects Band A of the counter, 300 MHz to 950 MHz.

(i) Band B (BB). This command selects Band B of the counter, 925 MHz to 18 GHz.

(j) Converter Auto (CA). This command selects the automatic sweep mode of the counter, and operates in conjunction with the YIG Preset (YP) command and value.

(k) Converter Manual (CM). This command selects the Manual mode of the counter, and operates in conjunction with YIG Preset (YP) command and value.

(m) Transmit Normal (TN). This command causes the counter to continuously transmit its reading when addressed to Talk.

(n) Transmit Service Request (TS). This command causes the counter to take a reading, format the data, store the result, and activate the SRQ line to indicate to the controller that a reading is ready for transmission. After the reading is transmitted, the SRQ line is deactivated and the process is repeated. The status byte transmitted during serial polling indicates that data is ready for transmission (bit 7 active).

NOTE

> Remote Resolution commands determine the resolution of the counter readings while in the Remote mode.

(p) Remote Resolution: 10 kHz (R4). Resolution of 10 kHz.

(q) Remote Resolution: 100 kHz (R5). Resolution of 100 kHz.

(r) Remote Resolution: 1 MHz (R6). Resolution of 1 MHz.

(s) Fast Active (FA). The FA command causes the counter to go into the fast cycle mode of operation. In this mode, the front-panel SAMPLE RATE control is inactive, and the fastest sample rate transmissions are attained.

(t) Fast Passive (FP). This command terminates FA.

(u) Exponent-Scientific (ES). This command causes the counter to output data in an engineering notation format if counter is addressed to Talk.

(v) Exponent-Four (E4). This command causes the counter to provide data in four exponent format if counter is addressed to Talk.

f. Output Data Format.

(1) Basic Format.

(a) The output data is transmitted with the most significant byte first, in a bit-parallel, byte-serial form, and in 7-bit ASCII code. The general format is

xx.xxx xx Ey CR LF

where CR is Carriage Return, LF is Line Feed, x represents digits 1 through 9, and y the exponent 0, 3, 6, or 9. The decimal point will be located in the proper place, though it may be deleted depending on the data output format and/or the reading.

(b) There will always be 12 bytes of information transmitted per reading. Leading zeros are always replaced with ASCII code Null characters. The last four bytes transmitted are always

Ey CR LF

where y represents exponents 0, 3, 6, or 9, and CR and LF the ASCII codes used as delineators.

(c) The ASCII code character E is used to specify the exponent 0, 3, 6, or 9, depending upon the value and format of the reading. Thus the data output commands (E4 or ES) affect only the numeric portion and exponent value of the transmitted data.

(2) Exponent-Four Output (E4) Format.

(a) In the E4 format, the exponent value of the transmitted data will always be 4 with no decimal point inserted. The reading will be transmitted as seen on the counter's front-panel display, with the resolution of the reading dependent upon the front-panel switches or the remote resolution commands. The digits affected by the resolution setting are set to zero. Some examples in the E4 format are as follows, with N representing an ASCII Null character.

(b) Display reading: 11 234.56 MHz

| Resolution | Reading transmitted |
|---|---|
| 10 kHz | N1123456 E4 CR LF |
| 100 kHz | N1123450 E4 CR LF |
| 1 MHz | N1123400 E4 CR LF |

(c) Display reading: 434.56 MHz

| Resolution | Reading transmitted |
|---|---|
| 10 kHz | NNN43456 E4 CR LF |
| 100 kHz | NNN43450 E4 CR LF |
| 1 MHz | NNN43400 E4 CR LF |

(3) Exponent-Scientific Output (ES) Format.

(a) In the ES format, the exponent value of the transmitted data is always 0, 3, 6, or 9, depending on the frequency reading. A decimal point is entered to correspond to the exponent so the transmitted data will be a mixed number of whole and fractional parts, such as 545.727, 15.72, 5.2, etc.

(b) All leading zeros are transmitted as ASCII Null characters, and the digits which are affected by the remote resolution are disregarded. (Null characters are inserted at the beginning of the data so that 12 characters are always transmitted.)

(c) If the resolution or frequency reading includes a decimal point that is not necessary, the decimal point is disregarded and a Null character is inserted at the beginning of the data.

(d) If the resolution affects the whole part of the number being transmitted (no decimal point or fractional part), zeros are inserted for those numbers before being transmitted.

(e) If the resolution covers the entire number, then all Nulls are transmitted with the exponent value of the reading, so the user can tell by the exponent value the manner in which the resolution covered the reading. For example: 0 Hz is transmitted as NNNNNNN0E0 CR LF.

(f) When local resolution is used (by pressing the RESOLUTION switches on the counter front panel), those digits affected by the resolution are replaced by zeros. Examples in the ES format are:

1. Frequency input: 1 234.56 MHz

| Remote resolution | Reading transmitted |
|---|---|
| 10 kHz | N 1.23456 E9 CR LF |
| 100 kHz | NN 1.2345 E9 CR LF |
| 1 MHz | NNN 1.234 E9 CR LF |

2. Frequency input: .56 GHz

| Remote resolution | Reading transmitted |
|---|---|
| 10 kHz | NN 560.00 E6 CR LF |
| 1 MHz | NNNNN 560 E6 CR LF |

(g) Transmitted readings, as printed out on a printer, are shown below.

NOTE

Leading Null characters are not printed.

| Printer output | Frequency |
|---|---|
| 434.6E6 | 434 600 000 Hz |
| 11.7693E9 | 11 769 300 000 Hz |
| 539.99999E9 | 539 999 990 Hz |
| 0E0 | 0 Hz |
| E6 | ? but in MHz range |

g. Wake-up Conditions. The wake-up conditions of the counter for the On Line mode, after power is applied or commands SDC or DCL have been issued by the controller, are as follows:

(1) Signal lines of the data bus are in tri-state mode.

(2) Counter is in Local mode (REMOTE indicator not lighted).

(3) Counter has sampled ADDRESS SWITCHes 1 through 7.

(4) Counter is not addressed to Talk or Listen

(5) No YIG Preset ($\overline{\text{YP}}$).

(6) Transmit Normal (TN).

(7) Remote - Band B (BB).

(8) Remote - Hold Passive (HP).

(9) Remote - 1 ms Gate Time Passive (TP).

(10) Remote - Resolution: 10 kHz (R4).

(11) Remote - Fast Passive (FP).

(12) Remote - Exponent-Scientific (ES) format.

(13) Remote - Converter Auto (CA).

(14) Counter and converter have been reset.

h. Band A (300 - 950 MHz) Operation.

CAUTION

Peak power applied to BAND A input connector should be between -10 and +10 dBm for normal operation. Peak input must not exceed +27 dBm or damage to the counter may result, even if the counter is turned off.

(1) Perform the preliminary procedures of paragraph 2-7b.

(2) Press the POWER switch to turn off the counter.

(3) Select an address for the counter by setting the GPIB IEEE STD 488/1975 ADDRESS SWITCHes 1 through 5 (fig. 2-8) in accordance with table 2-7. Make sure that ADDRESS SWITCH 7 is set to 0.

(4) Connect the GPIB controller to counter with a GPIB cable and appropriate interface to the counter rear-panel GPIB IEEE STD 488/1975 connector.

(5) Press the POWER switch to turn on the counter.

(6) Apply power to the controller.

(7) Connect the signal source to the BAND A input connector.

(8) Program REN (Remote Enable) from the controller.

(9) Check that the counter front-panel REMOTE indicator lights.

(10) Program BA to select Band A. Execute.

(11) Select and program R4, R5, or R6 for the desired resolution. Execute.

(12) If the input signal level is high enough for counting, both the front-panel LEVEL and LOCK indicators will light.

(13) Turn the counter SAMPLE RATE control to provide the desired display update rate. The GATE indicator will flash in accordance with the sample rate. If the control is set to its switched HOLD position, the display will retain the last reading. If a new reading is desired, program CC to cycle counter. Execute.

(14) If the counter is in a remote location, the controller can override the counter SAMPLE RATE control to obtain a HOLD, retaining the last reading. To program a HOLD:

(a) Program HA (Hold Active). Execute.

(b) To remove the HA (same as switching the counter SAMPLE RATE control out of HOLD), program HP (Hold Passive) to terminate the Hold Active. Execute.

(15) Program GTL (Go To Local) control with ASCII SOH or with a controller-unique command as appropriate. Execute. The counter should now have the REMOTE indicator off and should be in the Local operation Off Line modes.

i. Band B (925 MHz - 18 GHz) Operation.

CAUTION

Peak power applied to the BAND B input connector should be within the following ranges for normal operation:

925 MHz - 10 GHz: -10 to +10 dBm
10 - 18 GHz: -5 to +10 dBm

The peak input power must not exceed +30 dBm or damage to the counter may result, even if the counter is turned off.

(1) Initial Procedures.

(a) Perform the preliminary procedures of paragraph 2-7b.

(b) Perform procedures of paragraph 2-15h, steps (2) through (9), except that in step (7) connect the signal source to the BAND B input connector.

(c) Program BB to select Band B. Execute.

(d) Select and program R4, R5, or R6 for the desired resolution. Execute.

(e) If the input signal level is high enough for counting, both the front-panel LEVEL and LOCK indicators will light. If the REDUCE SIGNAL indicator lights, the input signal power is approaching the maximum safe operating level and should be reduced.

(2) Automatic Mode. In the automatic mode, the counter searches for the input signal by sweeping from a start frequency which is 105 MHz above a preset frequency.

(a) Program CA (Converter Auto). Execute.

NOTE

For full search, YP (YIG Preset) is not programmed, which is equivalent of setting the START SWEEP thumbwheel switches to 00.0 GHz.

(b) To improve acquisition speed, the sweep start frequency may be set by programming YP (YIG Preset) followed by a number. The lowest frequency which can then be acquired and displayed or recorded will be 105 MHz above the YIG Preset; erroneous readings may be displayed or recorded if the applied signal frequency is less than 105 MHz above the YIG Preset.

(c) To set the sweep start frequency equivalency of thumbwheel settings, program YP followed by a value and scale factor. Example: for a start frequency of 1.2 GHz, program YP 1.2 G (mnemonic YP, value 1.2, scale factor G). Execute.

(d) To reset the YIG Preset frequency to 00.0 GHz, program YP G (leaving out the value). Execute.

NOTE

To change the YIG Preset frequency from one value to another, or before resending the same value, YP must be set back to 00.0 GHz and the preset frequency programmed.

(e) Adjust the SAMPLE RATE control or program as described in paragraph 2-15h, steps (13) through (15).

(3) Manual Mode. In the manual mode, the search sweep is inhibited, reducing the acquisition time. However, the signal frequency to be measured must be between 105 and 325 MHz above the preset frequency.

(a) Program CM (Converter Manual). Execute.

(b) Program YIG Preset, Value, and Scale Factor to the desired frequency which must be 105 MHz to 325 MHz lower than the signal frequency. Example: if the expected measurement frequency is 12.35 GHz, program YP 12.2 G (which places the input frequency 105 to 325 MHz above the preset frequency). Execute.

NOTE

Erroneous readings may be displayed or recorded if the applied signal frequency is outside of the preset range.

(c) Adjust the SAMPLE RATE control or program as described in paragraph 2-15h, steps (13) through (15).

j. Programming Example Using Calculator as Controller.

(1) A typical program, utilizing a Hewlett-Packard 9815 Calculator as a GPIB controller, is shown in table 2-9. The program sets the counter as follows:

(a) Band A (BA)
(b) Remote Resolution - 10 kHz (R4)
(c) 1 ms Gate Passive (TP)
(d) Hold Passive (HP)
(e) Fast Active (FA)
(f) Exponent-Scientific (ES)
(g) No YIG Preset (YPM)

(2) The program then instructs the counter to take frequency readings and

### Table 2-9. Typical Program Using Hewlett-Packard 9815 Calculator as Controller

| Program step | Command | Comment |
|---|---|---|
| 0000 | Clear | Clear counter |
| 0001 | CMD 5 | Controller to COMMAND mode |
| 0003 | @ | |
| 0004 | B | Set REN line active |
| 0005 | END | Clear COMMAND mode |
| 0006 | CMD 5 | Enter COMMAND mode |
| 0008 | U | Controller talk address |
| 0009 | . | |
| 0010 | 3 | Counter listen address |
| 0011 | Blank | Counter goes to data transfer mode |
| 0012 | B | Device dependent data starts here |
| 0013 | A | Counter set to Band A |
| 0014 | R | Resolution 4 |
| 0015 | 4 | |
| 0016 | T | 1 ms Gate Passive |
| 0017 | P | |
| 0018 | H | Hold Passive |
| 0019 | P | |
| 0020 | F | Fast Active |
| 0021 | A | |
| 0022 | E | Exponent-Scientific |
| 0023 | S | |
| 0024 | Y | Clear YIG Preset |
| 0025 | P | |
| 0026 | M | |

Table 2-9. Typical Program Using Hewlett-Packard 9815 Calculator as Controller - Continued

| Program step | Command | Comment |
|---|---|---|
| 0027 | END | End device dependent mode |
| 0028 | Clear | |
| 0029 | 1 | |
| 0030 | Enter | |
| 0031 | 1 | |
| 0032 | 9 | |
| 0033 | Read 5 | Read frequency |
| 0034 | Print | |
| 0035 | Go to 0028 | Repeat |
| 0036 | END | |

prints out the results. For an input frequency of 580.75 MHz, the print-out might appear as

```
580750000
580760000
580740000
580760000
580760000
580750000
```

(3) The character E and exponent values are not presented; however, this is entirely dependent on the controller. Although the information was sent, the controller formatted and printed the data in this form. The way in which output data may be interpreted, and how data is sent to the counter, is entirely dependent on the controller used.

(4) Programs may be written to display the entire data transmission. An example of such an output, in which the program sampled the frequency at different resolutions and printed the results, is

```
RESOLUTION SCAN

...............

      285.24E6
       285.1E6
         285E6
       285.2E6

...............

   OFFSET SHIFT

...............

           0E0
         900E3
         9.9E6
        99.9E6
       999.9E6
      9.9999E9
```

# CHAPTER 3
# OPERATOR AND ORGANIZATIONAL MAINTENANCE

## Section I. LUBRICATION

3-1. No lubrication is required for the counter.

## Section II. TROUBLESHOOTING PROCEDURES

3-2. Table 3-1 lists the common malfunctions which you may find during operation or maintenance of the counter. You should perform the tests/inspections and corrective actions in the order listed.

3-3. This manual cannot list all malfunctions that may occur, nor all tests or inspections and corrective actions. If a malfunction is not listed or is not corrected by listed corrective actions, notify your supervisor.

Table 3-1. Operator and Organizational Troubleshooting

MALFUNCTION
TEST OR INSPECTION
CORRECTIVE ACTION

1. No display - power not supplied to instrument.

    Step 1. Check if rear-panel fuse is blown.

        Replace fuse with fuse of proper rating for operating voltage: 1.5 A slow-blow for 115 Vac, or 0.75 A slow-blow for 230 Vac.

    Step 2. Check that power cable is seated in rear-panel mounted connector.

        Seat power cable connector.

    Step 3. Check power cable for open circuit and/or damaged connector blades.

        Replace power cable.

2. SAMPLE RATE control has no effect on display.

    Step 1. Check that rear-panel mounted STORAGE and MIN. PRF switches are both in down position.

        Set STORAGE switch to ON and MIN. PRF switch to 50 Hz.

    Step 2. Check GPIB IEEE STD 488/1975 ADDRESS SWITCHes.

        Set ADDRESS SWITCHes 1 and 2 to 0 position (top pushed in).

Table 3-1. Operator and Organizational Troubleshooting - Continued

MALFUNCTION
TEST OR INSPECTION
CORRECTIVE ACTION

Step 3. Check that REMOTE indicator is not lighted.

If REMOTE indicator is lighted and GPIB controller is connected, Fast Active (FA) may be in control. Program Fast Passive (FP) and execute on GPIB controller to remove Fast Active command. If programming and executing FP does not correct, Hold Active (HA) may be in control. Program Hold Passive (HP) and execute on GPIB controller to remove Hold Active command.

3. RESOLUTION selector switches do not change display with signal source(s) connected to input connector(s).

Step 1. Check that REMOTE indicator is not lighted.

If REMOTE indicator is lighted and GPIB controller is connected, resolution commands R4, R5, or R6 may be in control. Program Go To Local Control (GTL) and execute.

4. Display shows incorrect or erratic reading for BAND A inputs.

Step 1. Check that LEVEL indicator is lighted.

CAUTION

Do not exceed +10 dBm peak power input to the BAND A connector.

If not lighted, increase signal level until LEVEL indicator lights.

Step 2. Press BAND A pushbutton firmly. Cycle between BAND B and BAND A pushbuttons, ending up with BAND A.

Alternately selecting BAND A and BAND B pushbuttons may free up contacts.

5. Display shows erroneous reading for BAND B inputs.

Step 1. Check PRESET FREQUENCY thumbwheel switch settings if in MANUAL SELECT. Setting must be 105 to 325 MHz below input frequency.

Set thumbwheel switches to proper preset frequency.

Step 2. Check START FREQUENCY thumbwheel settings if in AUTO SWEEP mode. Setting must be at least 105 MHz below input frequency.

Set thumbwheel switches to proper start frequency.

Table 3-1. Operator and Organizational Troubleshooting - Continued

MALFUNCTION
TEST OR INSPECTION
CORRECTIVE ACTION

6. Counter does not count correctly with GPIB controller connected.

Step 1. Check that rear-panel ADDRESS SWITCH 7 is set to 0 (top pushed in).

Set ADDRESS SWITCH 7 to 0. Remove counter power and controller power. Wait five seconds, then press counter POWER pushbutton and apply power to GPIB controller. This should remove microprocessor lock-up so that GPIB controller can function.

## Section III. MAINTENANCE PROCEDURES

### 3-4. Introduction.

Operator and organizational maintenance is limited to inspection, exterior cleaning, fuse and power cable replacement, and performance of the counter self-test.

### 3-5. Inspection.

Inspection is accomplished by performing the preventive maintenance checks listed in table 2-3.

### 3-6. Cleaning.

Cleaning instructions appear in paragraph 2-5.

### 3-7. Replacement.

a. Fuse. Replace a blown fuse as follows:

(1) Disconnect power cable at rear of counter and slide plastic fuse cover over power connector.

CAUTION

The FUSE PULL lever attached to the body of the power module housing does not come off. Firm but careful rotation of the fuse puller will lift up one end of the fuse so that finger force can remove the fuse. Failure to heed this caution by exerting too much force may damage the plastic pivot of the built-in fuse puller.

(2) Remove installed fuse by lifting up on FUSE PULL lever.

(3) Visually inspect fuse, or check with an ohmmeter, to confirm that it is blown.

(4) Reinstall original fuse (if not blown) or replace defective fuse with one of proper rating: 1.5 A slow-blow for 115 Vac, 0.75 A slow-blow for 230 Vac.

(5) Slide fuse cover over fuse and reconnect power cable to connector.

b. Power Cable. If the power cable is frayed or damaged, it must be replaced.

### 3-8. Test.

After each maintenance action, the counter must be tested in accordance with the procedures in paragraph 2-7b.

# CHAPTER 4
# DIRECT SUPPORT AND GENERAL SUPPORT MAINTENANCE

## Section I. REPAIR PARTS, SPECIAL TOOLS; TEST, MEASUREMENT, AND DIAGNOSTIC EQUIPMENT (TMDE); AND SUPPORT EQUIPMENT

4-1. Common Tools and Equipment.

For authorized common tools and equipment, refer to the Modified Table of Organization and Equipment (MTOE) applicable to your unit.

4-2. Special Tools, TMDE, and Support Equipment.

No special tools are required. TMDE and support equipment are listed in the Maintenance Allocation Chart, Appendix B of this manual.

4-3. Repair Parts.

Repair parts are listed and illustrated in the repair parts and special tools list, TM 11-6625-3031-24P, covering direct support and general support maintenance for this equipment.

## Section II. SERVICE UPON RECEIPT

4-4. Upon receipt of the pulse counter and prior to performing maintenance follow the assembly and preparation for use instructions in paragraph 2-6. Become familiar with the control settings and indicators by reviewing the operating instructions starting with paragraph 2-7. Then proceed with the following troubleshooting instructions.

## Section III. TROUBLESHOOTING

4-5. Introduction.

a. Table 4-1, a symptom index, is provided so that you can match what is observed on the counter with the symptom index and, from there, go to the page in the troubleshooting table which covers the malfunction. Use of the counter operating controls and display observation constitutes the initial troubleshooting, followed by measurements of increasing complexity.

b. Standard troubleshooting practice should start with the obvious, for example: blown fuses, power and signal connections, improper seating or poor connection of cables, etc. After these basic troubleshooting practices have eliminated the obvious, then disassembly or cover removal of the counter should be considered.

SAFETY PRECAUTION

A periodic review of safety precautions in TB 385-4, Safety Precautions for Maintenance of Electrical/Electronic Equipment, is recommended. When the equipment is operated with covers removed, DO NOT TOUCH exposed connections or components. MAKE CERTAIN you are not grounded when making connections or adjusting components.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of performing first aid, is present.

c. The troubleshooting table lists the common malfunctions which you may find during the operation or maintenance of the counter or its components. You should perform the tests/inspections and corrective actions in the order listed.

d. This manual cannot list all malfunctions that may occur, nor all tests or inspections and corrective actions. If a malfunction is not listed or is not corrected by listed corrective actions, notify your supervisor.

NOTE

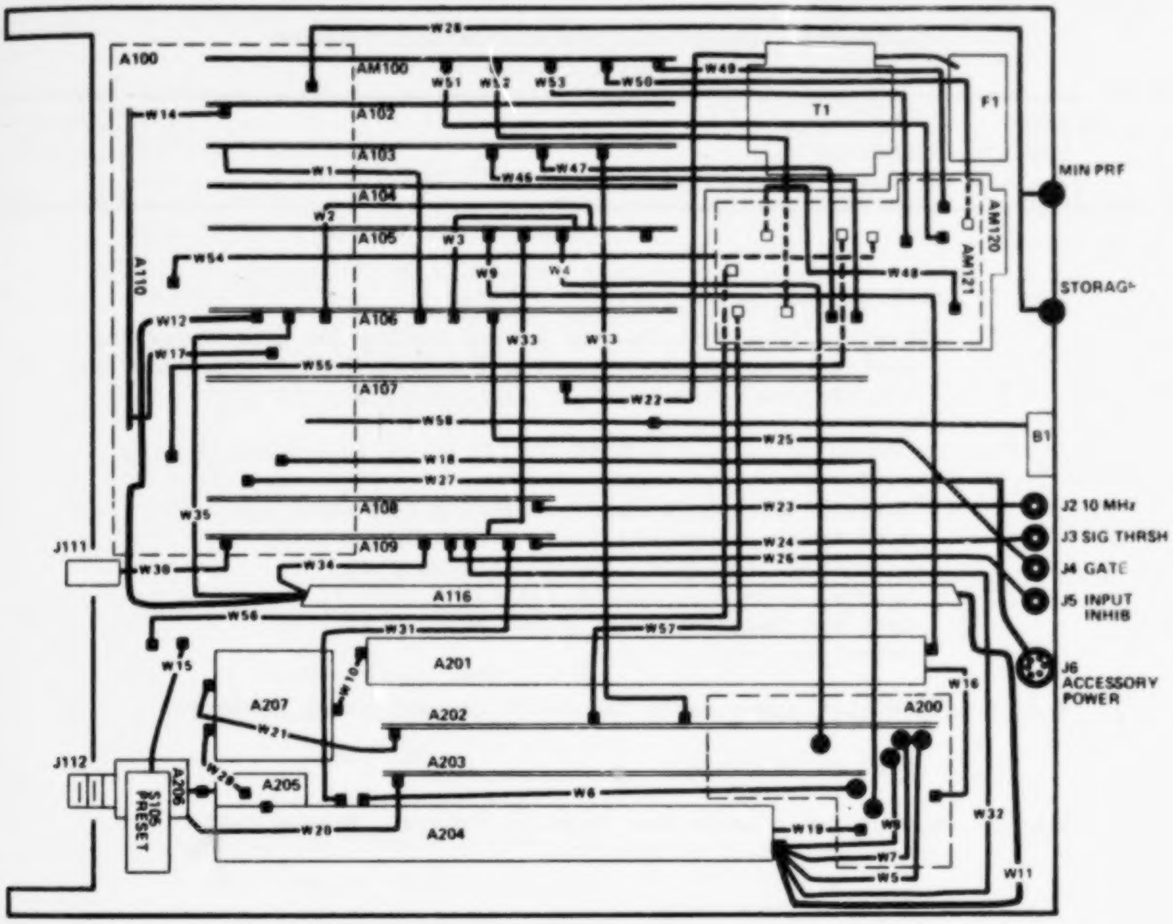
General Purpose Interface Bus (GPIB) troubleshooting procedures are in the depot maintenance work requirements, CECOM DMWR 11-6625-3031, for this equipment.

4-6. Reference Diagrams.

Block diagrams are shown in fig. 1-2, 1-3, and 1-4. Subassembly and cable locations are shown in fig. 4-1. Fold-out schematic diagrams are located in the rear of this manual.

Table 4-1. Symptom Index

| Symptom | Troubleshooting procedure page |
|---|---|
| 1. Display | 4-4 |
| No zeros | 4-4 |
| Display does not indicate 88 888.88 when TEST DISPLAY pushbutton is pressed | 4-6 |
| Display does not indicate 200 MHz when TEST 200 MHz pushbutton is pressed | 4-6 |
| Missing digit | 4-7 |
| Band A incorrect reading | 4-8 |
| Band B incorrect reading | 4-10 |
| 2. LED Indicators | 4-13 |
| LEVEL indicator does not light. | 4-13 |
| LEVEL indicator blinks or lights continuously without Band B input signal | 4-14 |
| LOCK indicator does not light | 4-15 |
| LOCK indicator blinks or lights continuously without Band B input signal | 4-15 |
| GATE indicator does not light | 4-15 |
| REDUCE SIGNAL indicator does not light | 4-16 |


W28
A100
AM100
W51
W52
W53
W50
W49
T1
F1
W14
A102
A103
W1
W46
W47
A104
W2
A105
W3
W9
W4
W54
A110
AM120
AM121
W48
MIN PRF
STORAGE
W12
A106
W17
W33
W13
W55
A107
W22
W58
B1
W25
W18
W27
A108
W23
J2 10 MHz
J3 SIG THRSH
J4 GATE
J5 INPUT INHIB
W35
J111
A109
W24
W26
W30
W34
A116
W56
W31
W57
W15
A201
J6 ACCESSORY POWER
W10
A207
W16
A200
A202
W21
J112
A206
S105 PRESET
W29
A205
A203
W6
W20
A204
W19
W8
W32
W7
W5
W11

## CABLE INTERCONNECTIONS

| | | |
|---|---|---|
| A103P2 | W1 | A106J5 |
| A105P2 | W2 | A106J1 |
| A105P3 | W3 | A106J4 |
| A200P2 | W4 | A105J1 |
| A200P3 | W5 | A204J6 |
| A200P4 | W6 | A204J2 |
| A200P5 | W7 | A204J7 |
| A200P6 | W8 | A204J4 |
| A201J1 | W9 | A105J4 |
| A201J2 | W10 | A207J2 |
| A116 DELAY | W11 | A204J3 |
| | W12 | A106J3 |
| A103J3 | W13 | A202J2 |
| A110P2 | W14 | A102J1 |
| A1P121 | W15 | A100J6 |
| A201P1 | W16 | A200J2 |
| A110P1 | W17 | A100J2 |
| A200P1 | W18 | A100J3 |
| A204P1 | W19 | A200J1 |
| A206P2 | W20 | A203J1 |
| A202J3 | W21 | (A2)Q1<br>A207J3 |
| A1(T1)P101 | W22 | A107J1 |
| (AI)P102(J2) | W23 | A108J1 |
| (A1)P103(J3) | W24 | A109J6 |
| (A1)P104(J4) | W25 | A106J6 |
| (A1)P105(J5) | W26 | A109J3 |
| (A1)P106(J6) | W27 | A100J8 |
| (A1)P107 | W28 | A100J1 |
| A205P1 | W29 | A207J1 |
| A1J111 | W30 | A109J1 |
| A204J1 | W31 | A109J5 |
| A204J5 | W32 | A109J4 |
| A105J2 | W33 | A109P2 |
| A116 DELAY | W34 | A109J2 |
| | W35 | A106J2 |
| AM120J1 | W46 | A103J2 |
| AM120J2 | W47 | A103J1 |
| AM120J3 | W48 | AM121J2 |
| AM120J4 | W49 | AM100J2 |
| AM121J1 | W50 | AM100J3 |
| AM120J5 | W51 | AM100J6 |
| AM121J5 | W52 | AM100J5 |
| AM120J6 | W53 | AM100J4 |
| AM121J3 | W54 | A100J4 |
| AM121J4 | W55 | A100J5 |
| AM121J6 | W56 | A100J7 |
| AM121J7 | W57 | A202J1 |
| A100P1 | W58 | (A1)B1J1 |

EL80Y013

Figure 4-1. Subassembly and Cable Locations

Table 4-2. Direct Support and General Support Troubleshooting

---

MALFUNCTION
TEST OR INSPECTION
CORRECTIVE ACTION

---

1. No zeros.

Step 1. Check if rear-panel fuse F1 is blown.

Replace fuse with fuse of proper rating for line operating voltage: 1.5 A slow-blow for 115 Vac, 0.75 A slow-blow for 230 Vac.

NOTE

While inspecting fuse or replacing fuse make sure that appropriate line voltage is visible on voltage selector card under fuse post housing. Card should be seated so that it does not interfere with slide protective cover.

Step 2. Check that power cable is seated in rear-panel connector.

Seat power cable.

Step 3. Inspect power cable for physical damage. Remove cable from counter and check continuity.

Replace power cable.

Step 4. Check that following cables are seated properly at both ends:

W22 from transformer T1 to Power Supply A107.

W17 from Display A110 to Counter Interconnect A100.

W14 from Display A110 to Count Chain Control A102.

W46 from Count Chain A103 to GPIB BCD Output AM120.

W47 from Count Chain A103 to GPIB BCD Output AM120.

W1 from Count Chain A103 to High Frequency A106.

Seat cable connections.

Step 5. Place rear-panel MIN. PRF switch in 50 Hz position and STORAGE switch in ON position. Press and release front-panel RESET pushbutton. If zeros now appear on display, Control A104 may be faulty.

Remove and replace Control A104.

Step 6. Check cables W1, 46, and W47 for opens or shorts.

Replace defective cable.

Table 4-2. Direct Support and General Support Troubleshooting - Continued

MALFUNCTION
TEST OR INSPECTION
CORRECTIVE ACTION

Step 7. Check continuity of cables:

W17 and W14 from Display A110.

If open or shorted, replace Display A110.

W22 from transformer T1.

If open or shorted, replace transformer T1.

Step 8. Disconnect cable W27 from J8 on Counter Interconnect A100 (fig. 4-2). Measure dc voltages between ground and pins of J8, which should be +5 V at pin 1, -5.2 V at pin 2, +12 V at pin 3, and -12 V at pin 4.

If one or more voltages are not as specified, proceed to step 9. If all voltages are normal, remove and replace the following circuit cards in sequence specified:

Count Chain Control A102

Count Chain A103

Control A104

Gate Generator A105

High Frequency A106

Display A110

GPIB Remote/Local Control AM121

GPIB BCD Output AM120.

Step 9. Same as step 8.

Disconnect all circuit cards and cables, one at a time, until abnormal voltage(s) are restored to correct level. Replace defective circuit card or module which caused fault.

Step 10. Disconnect cable W22 from A107J1. Check for ac voltages on cable connector: 18 volts ac between pin 1 (brown wire) and pin 2 (red wire), 9 volts ac between pin 4 (yellow wire) and pin 5 (green wire). If ac voltages are normal, Power Supply A107 may be faulty.

Replace Power Supply A107.

Step 11. Remove protective cover from power module (31, fig. 4-3) and check for following ac voltages on power module: pins F to D, 115 volts ac; pins E to C, 115 volts ac. If ac voltages are normal, transformer T1 may be faulty.

Replace transformer assembly.

Table 4-2. Direct Support and General Support Troubleshooting - Continued

MALFUNCTION
TEST OR INSPECTION
CORRECTIVE ACTION

Step 12. Check for following ac voltages on power module: pins J to B, 115 volts ac; pins L to N, 115 volts ac. If ac voltage on pins L and N is normal, and pushing and releasing POWER switch several times does not place 115 volts on pins J and B, POWER switch is faulty.

Replace POWER switch S101.

2. Display does not indicate 88 888.88 when TEST DISPLAY pushbutton is pressed.

Step 1. Remove and replace Count Chain Control A102. If 88 888.88 now appears on display when TEST DISPLAY pushbutton is pressed, original A102 was defective.

Replace Count Chain Control A102.

Step 2. Using card extender, elevate Count Chain Control A102 from Counter Interconnect A100. Jumper pins E and A on A102P1. If 88 888.88 now appears on display, TEST DISPLAY switch S2 on Counter Interconnect A100 may be defective.

Replace Counter Interconnect A100.

Step 3. Check that cables W14 from Display A110 to Count Chain Control A102 and W17 from Display A110 to Counter Interconnect A100 are firmly seated.

Seat cable connections.

Step 4. Check continuity of following cables:

W17 from Display A110.

If open or shorted, replace Display A110.

W14 from Display A110.

If open or shorted, replace Display A110.

3. Display does not indicate 200 MHz when TEST 200 MHz pushbutton is pressed.

Step 1. Remove and replace following circuit cards in sequence to fault isolate by substitution. After each substitution, press TEST 200 MHz switch and check display.

Control A104
Reference Oscillator Buffer A108
High Frequency A106
Gate Generator A105
Count Chain A103

Table 4-2. Direct Support and General Support Troubleshooting - Continued

MALFUNCTION
TEST OR INSPECTION
CORRECTIVE ACTION

Count Chain Control A102

Source/Amplifier A201.

Replace defective circuit card.

Step 2. Ground pin 1 of TEST 200 MHz switch A100S1 (fig. 4-2). If 200 MHz now shows on display, switch may be defective.

Replace Counter Interconnect A100.

Step 3. Check that following cables are seated properly at both ends:

W18 from Counter Interconnect A100 to Converter Interconnect A200.

W9 from Source/Amplifier A201 to Gate Generator A105.

W2 from Gate Generator A105 to High Frequency A106.

W3 from Gate Generator A105 to High Frequency A106.

W1 from High Frequency A106 to Count Chain A103.

W14 from Display A110 to Count Chain Control A102.

Seat cable connections.

Step 4. Check cables listed in step 3.

If W9 is open or shorted, replace cable.

If W18 is open or shorted, replace Converter Interconnect A200.

If W2 is open or shorted, replace Gate Generator A105.

If W3 is open or shorted, replace Gate Generator A105.

If W1 is open or shorted, replace Count Chain A103.

If W14 is open or shorted, replace Display A110.

4. Missing digit.

Step 1. Remove and replace the following circuit cards in sequence to fault isolate by substitution.

Count Chain Control A102

GPIB Remote/Local Control AM121

GPIB BCD Output AM120

Display A110

Replace defective circuit card.

## Table 4-2. Direct Support and General Support Troubleshooting - Continued

MALFUNCTION
TEST OR INSPECTION
CORRECTIVE ACTION

Step 2. Ground pin 1 on RESOLUTION switches A100S3 and A100S4 (fig. 4-2). Display will not show last two digits. Unground pin 1 on switches A100S3 and A100S4 in sequence. Digits should appear as ground is removed.

Replace Counter Interconnect A100.

Step 3. Check that following cables are seated properly at both ends.

W14 from Display A110 to Count Chain Control A102.

W54 from Interconnect A100 to GPIB Remote/Local Control AM121.

W55 from Interconnect A100 to GPIB Remote/Local Control AM121.

W48 from GPIB Remote/Local Control AM121 to GPIB BCD Output AM120.

Seat cable connections.

Step 4. Check cables W48, W54, and W55 for opens or shorts.

Replace defective cable.

Step 5. Check cable W14 from Display A110.

If open or shorted, replace Display A110.

5. Band A incorrect reading.

Step 1. Check that rear-panel MIN. PRF switch is in 50 Hz position and STORAGE switch is in ON position.

Place switches in correct positions.

Step 2. Check that input signal is connected to Band A connector and that BAND A selector switch is pressed in.

Connect and operate appropriately.

Step 3. Check input signal frequency and level. Must be between 300 and 950 MHz at level between -10 dBm and +10 dBm.

Adjust input frequency and level.

Step 4. If GPIB controller is connected to counter, check that REMOTE indicator is not lighted. If lighted, GPIB program commands are controlling counter.

Program Go To Local (GTL) from controller and execute to return counter to local mode operation.

Step 5. Check that LEVEL and LOCK indicators are lighted and GATE indicator flashes at rate determined by SAMPLE RATE control setting.

Replace Control A104.

Table 4-2. Direct Support and General Support Troubleshooting - Continued

MALFUNCTION
TEST OR INSPECTION
CORRECTIVE ACTION

Step 6. Check gate accuracy; see paragraph 4-8c.

Adjust as required.

Step 7. Remove and replace following circuit cards in sequence to fault isolate by substitution:

Control A104
Prescaler A109
Reference Oscillator Buffer A108
Gate Generator A105
High Frequency A106
Count Chain Control A102
Count Chain A103
Dual Delay Line A116
GPIB Remote/Local Control AM121.

Replace defective circuit card.

NOTE

If High Frequency A106 card is replaced, adjust in accordance with paragraph 4-8c.

Step 8. Check that following cables are seated properly at both ends:

W30 from BAND A connector A1J111 to Prescaler A109.
W34 from Prescaler A109 to Dual Delay Line A116.
W35 from Dual Delay Line A116 to High Frequency A106.
W33 from Prescaler A109 to Gate Generator A105.
W3 from Gate Generator A105 to High Frequency A106.
W1 from High Frequency A106 to Count Chain A103.
W54 from GPIB Remote/Local Control AM121 to Counter Interconnect A100.
W55 from GPIB Remote/Local Control AM121 to Counter Interconnect A100.

Seat cable connections.

Step 9. Check cables W30, W54, and W55 for opens or shorts.

Replace defective cable.

Table 4-2. Direct Support and General Support Troubleshooting - Continued

MALFUNCTION
TEST OR INSPECTION
CORRECTIVE ACTION

Step 10. Check following cables:

W34 from Dual Delay Line A116

If open or shorted, replace Dual Delay Line A116.

W35 from Dual Delay Line A116

If open or shorted, replace Dual Delay Line A116.

W33 from Prescaler A109

If open or shorted, replace Prescaler A109.

W3 from Gate Generator A105

If open or shorted, replace Gate Generator A105.

W1 from Count Chain A103

If open or shorted, replace Count Chain A103.

6. Band B incorrect reading.

Step 1. Check that rear-panel MIN. PRF switch is in 50 Hz position and STORAGE switch is in ON position.

Place switches in correct positions.

Step 2. Check that input signal is connected to BAND B connector and that BAND B selector switch is pressed in.

Connect and operate appropriately

Step 3. Check input signal frequency and level. Must be between 925 MHz and 18 GHz, with levels as follows: 925 MHz to 10 GHz, between -10 dBm and +7 dBm; 10 to 18 GHz, between -5 dBm and +7 dbm.

Adjust input frequency and level.

Step 4. Check that MANUAL SELECT/AUTO SWEEP switch is set to AUTO SWEEP and START FREQUENCY thumbwheel switches are set to 00.0 GHz.

Place switches in proper positions.

Step 5. Check that REDUCE SIGNAL indicator is not lighted or only flashes occasionally.

Reduce signal level.

Step 6. If GPIB controller is connected to counter, check that REMOTE indicator is not lighted. If lighted, GPIB program commands are controlling counter.

Table 4-2. Direct Support and General Support Troubleshooting - Continued

MALFUNCTION
TEST OR INSPECTION
CORRECTIVE ACTION

Program Go To Local (GTL) from controller and execute to return counter to local mode operation.

Step 7. Check that LEVEL and LOCK indicators are lighted and GATE indicator flashes at rate determined by SAMPLE RATE control setting.

Replace Control A104.

Step 8. Check counter adjustments; see paragraph 4-8.

Adjust as required.

Step 9. Remove and replace following in sequence to fault isolate by substitution:

Control A104
Reference Oscillator Buffer A108
Prescaler A109
Count Chain Control A102
Count Chain A103
Gate Generator A105
High Frequency A106
Converter Sequencer A203
YIG Control A202
GPIB BCD Output AM120
GPIB Remote/Local Control AM121
Dual Delay Line A116
Source/Amplifier A201
Limiter/Attenuator A206
I.F. Processor A204
YIG Comb Generator A207.

Replace defective assembly.

NOTE

Adjustments specified in paragraph 4-8 are required if any of the following are replaced:

High Frequency A106
YIG Control A202

Table 4-2. Direct Support and General Support Troubleshooting - Continued

MALFUNCTION
TEST OR INSPECTION
CORRECTIVE ACTION

---

Converter Sequencer A203

I.F. Processor A204

Source/Amplifier A201

Limiter/Attenuator A206

YIG Comb Generator A207

If Reference Oscillator Buffer A108 is replaced, recalibration is required.

Step 10. Check that following cables are seated properly at both ends:

W1 from Count Chain A103 to High Frequency A106.
W3 from Gate Generator A105 to High Frequency A106.
W4 from Converter Interconnect A200 to Gate Generator A105.
W5 from Converter Interconnect A200 to I.F. Processor A204.
W6 from Converter Interconnect A200 to I.F. Processor A204.
W7 from Converter Interconnect A200 to I.F. Processor A204.
W8 from Converter Interconnect A200 to I.F. Processor A204.
W9 from Source/Amplifier A201 to Gate Generator A105.
W10 from Source/Amplifier A201 to YIG Comb Generator A207.
W11 from I.F. Processor A204 to Dual Delay Line A116.
W12 from Dual Delay Line A116 to High Frequency A106.
W13 from YIG Control A202 to Count Chain Control A102.
W14 from Count Chain Control A102 to Display A110.
W15 from thumbwheel switch to Counter Interconnect A100.
W16 from Source/Amplifier A201 to Converter Interconnect A200.
W17 from Display A110 to Counter Interconnect A100.
W18 from Counter Interconnect A100 to Converter Interconnect A200.
W19 from Converter Interconnect A100 to I.F. Processor A204.
W20 from Limiter/Attenuator A206 to Converter Sequencer A203.
W21 from YIG Control A202 to YIG Comb Generator A207.
W29 from YIG Comb Generator to Mixer A205.
W31 from I.F. Processor A204 to Prescaler A109.
W54 from Counter Interconnect A100 to GPIB Remote/Local Control AM121.

Table 4-2. Direct Support and General Support Troubleshooting - Continued

MALFUNCTION
TEST OR INSPECTION
CORRECTIVE ACTION

W55 from GPIB Remote/Local Control AM121 to Counter Interconnect A100.

W56 from Counter Interconnect A100 to GPIB Remote/Local Control AM121.

Seat cable connections.

Step 11. Check following cables:

W9, W10, W13, W21, W31, W54, W55, W56, and W29 for opens or shorts.

Replace defective cable.

Step 12. Check following cables:

W1 from Count Chain A103.

If open or shorted, replace Count Chain A103.

W3 from Gate Generator A105.

If open or shorted, replace Gate Generator A105.

W4, W5, W6, W7, and W8 from Converter Interconnect A200.

If open or shorted, replace Converter Interconnect A200.

W11 and W12 from Dual Delay Line A116.

If open or shorted, replace Dual Delay Line A116.

W14 and W17 from Display A110.

If open or shorted, replace Display A110.

W15 from thumbwheel switch assembly.

If open or shorted, replace thumbwheel switch assembly.

W16 from Source/Amplifier A201.

If open or shorted, replace Source/Amplifier A201.

W19 from I.F. Processor A204.

If open or shorted, replace I.F. Processor A204.

W20 from Limiter/Attenuator A206.

If open or shorted, replace Limiter/Attenuator A206

7. LEVEL indicator does not light.

Step 1. Check level of input signal with power meter/thermistor mount. Input level must be above -10 dBm for frequencies between 300 MHz and 10 GHz, and above -5 dBm for frequencies between 10 and 18 GHz.

### Table 4-2. Direct Support and General Support Troubleshooting - Continued

MALFUNCTION
TEST OR INSPECTION
CORRECTIVE ACTION

Increase level of input signal, but not above +10 dBm between 300 MHz and 10 GHz, nor above +7 dBm between 10 to 18 GHz.

Step 2. Check for +5 Vdc on pin 1 of W17P1, then jumper pin 6 (ground) to pin 2. LEVEL indicator should light.

Replace Display A110.

Step 3. Remove and replace following in sequence to fault isolate by substitution.

Control A104

Gate Generator A105

Prescaler A109 (if Band A inputs do not light LEVEL indicator)

I.F. Processor A204 (if Band B inputs do not light LEVEL indicator).

Replace defective assembly.

Step 4. Check that following cables are seated properly at both ends:

W17 from Display A110 to Counter Interconnect A100

W33 from Prescaler A109 to Gate Generator A105

W4 from Converter Interconnect A200 to Gate Generator A105

W5 from Converter Interconnect A200 to I.F. Processor A204.

Seat cable connections.

Step 5. Check following cables:

W17 from Display A110.

If open or shorted, replace Display A110.

W33 from Prescaler A109.

If open or shorted, replace Prescaler A109.

W4 and W5 from Converter Interconnect A200.

If open or shorted, replace Converter Interconnect A200.

8. LEVEL indicator blinks or lights continuously without Band B input signal.

Step 1. Adjust in accordance with paragraphs 4-8d through f.

Replace Converter Sequencer A203.

Step 2. Repeat step 1.

Replace YIG Control A202.

Table 4-2. Direct Support and General Support Troubleshooting - Continued

---

MALFUNCTION
TEST OR INSPECTION
CORRECTIVE ACTION

---

9. LOCK indicator does not light.

Step 1. Check for +5 Vdc on pin 1 of W17P1, then jumper pin 6 (ground) to pin 3. LOCK indicator should light.

Replace Display A110.

Step 2. Remove and replace following in sequence to fault isolate by substitution:

Control A104

Converter Sequencer A203

I.F. Processor A204.

Replace defective assembly.

Step 3. Check that following cables are seated properly at both ends:

W17 from Display A110 to Counter Interconnect A100.

W18 from Converter Interconnect A200 to Counter Interconnect A100.

W7 from Converter Interconnect A200 to I.F. Processor A204.

Seat cable connections.

Step 4. Check following cables:

W17 from Display A110.

If open or shorted, replace Display A110.

W7 and W18 from Converter Interconnect A200.

If open or shorted, replace Converter Interconnect A200.

10. LOCK indicator blinks or lights continuously without Band B input signal.

Step 1. Adjust in accordance with paragraphs 4-8d through f.

Replace Converter Sequencer A203.

Step 2. Repeat step 1.

Replace YIG Control A202.

11. GATE indicator does not light.

Step 1. Check for +5 Vdc on pin 1 of W17P1, then jumper pin 6 (ground) to pin 4. GATE indicator should light.

Replace Display A110.

### Table 4-2. Direct Support and General Support Troubleshooting - Continued

MALFUNCTION

TEST OR INSPECTION

CORRECTIVE ACTION

Step 2. Remove and replace following in sequence to fault isolate by substitution:

Control A104

Count Chain Control A102

Gate Generator A105.

Replace defective assembly.

Step 3. Check that cable W17, between Display A110 and Counter Interconnect A100, is seated properly.

Seat cable connections.

Step 4. Check cable W17.

If open or shorted, replace Display A110.

12. REDUCE SIGNAL indicator does not light.

NOTE

This indicator functions only on Band B inputs and should light when input power approaches the maximum safe operating level.

Step 1. Check for approximately +0.5 Vdc on pin 14 of connector on W15.

Replace REDUCE SIGNAL indicator DS101 if voltage is present.

Step 2. Remove and replace following in sequence to fault isolate by substitution:

YIG Control A202

Converter Sequencer A203

GPIB Remote/Local Control AM121.

Step 3. Check that following cables are seated properly at both ends:

W15 from thumbwheel switch assembly to Counter Interconnect A100.

W56 from Counter Interconnect A100 to GPIB Remote/Local Control AM121.

W57 from GPIB Remote/Local Control AM121 to YIG Control A202.

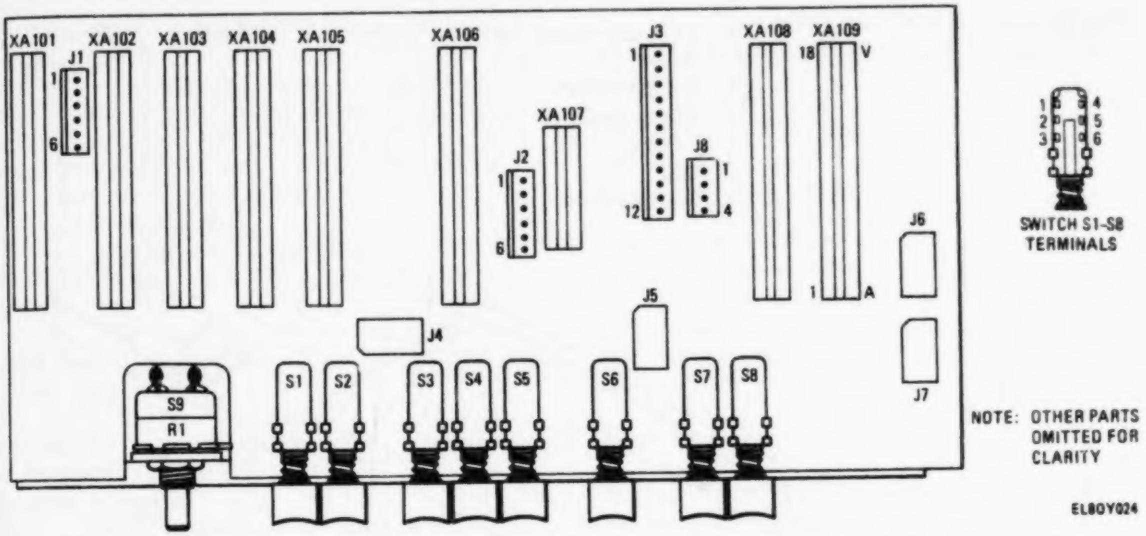
Seat cable connections.

Step 4. Check cables W56 and W57 for opens or shorts.

Replace defective cable.

Step 5. Check cable W15 from thumbwheel switch assembly.

If open or shorted, replace thumbwheel switch assembly.



NOTE: OTHER PARTS OMITTED FOR CLARITY

EL80Y024

Figure 4-2. Counter Interconnect A100, Connector and Switch Locations

## Section IV. MAINTENANCE PROCEDURES

### 4-7. Disassembly, Replacement, and Reassembly.

a. General Instructions. Access to the interior of the counter is obtained by removing the top and/or bottom covers. Each cover may be removed by loosening the four screws which secure it to the counter frame. Circuit cards are held in place by a retainer (22, fig. 4-3) which is secured by six screws (20) and lockwashers (21).

WARNING

Before proceeding with any further disassembly, be sure the counter is disconnected from the ac power source. Voltages as high as 230 Vac may exist in the counter. Serious injury or DEATH may result from contact with these potentials.

CAUTION

Always use an IC extractor to disconnect ribbon cables to prevent damage to the connectors.

b. GPIB Circuit Cards AM120 and AM121. Circuit cards AM120 and AM121 must be removed from and reassembled in the counter as a single assembly, although either may be replaced in the event of failure.

(1) Disassembly.

(a) Remove the top and bottom covers from the counter.

(b) Remove six screws (20, fig. 4-3) and lockwashers (21) securing retainer (22), and remove the retainer.

(c) Disconnect the ribbon cables from AM120 (51) and AM121 (9).

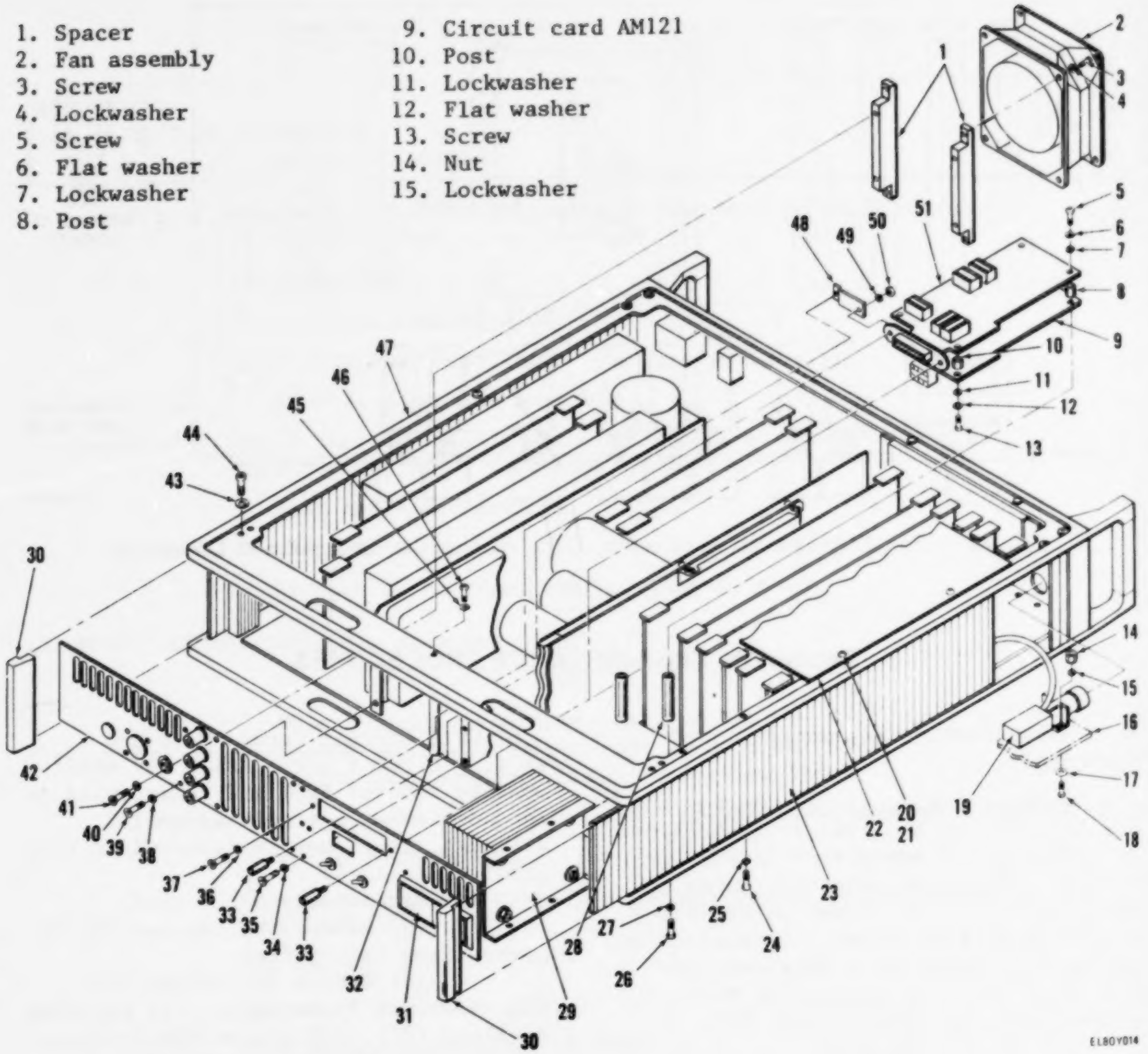
(d) Remove screw (37), lockwasher (36), two studs (33), three nuts (50), and three lockwashers (49) which secure circuit card AM120 (51) and adapter (48) to rear panel assembly (42).

(e) Remove two screws (26) and lockwashers (27) which secure posts (28) to the frame.

(f) Pull assembled circuit cards away from the rear panel and out of the top of the counter.

(g) Remove two screws (5), flat washers (6), and lockwashers (7)

1. Spacer
2. Fan assembly
3. Screw
4. Lockwasher
5. Screw
6. Flat washer
7. Lockwasher
8. Post
9. Circuit card AM121
10. Post
11. Lockwasher
12. Flat washer
13. Screw
14. Nut
15. Lockwasher


2
1
3
4
5
6
7
48
49
50
51
8
9
10
11
12
13
47
46
45
44
43
30
14
15
16
17
18
19
20
21
22
23
42
41
40
39
38
37
36
33
35
34
33
32
31
30
29
28
27
26
25
24
ELBOY014

16. Circuit card A100
17. Flat washer
18. Screw
19. POWER switch
20. Screw
21. Lockwasher
22. Retainer
23. Side panel
24. Screw
25. Lockwasher
26. Screw
27. Lockwasher
28. Post
29. Transformer assembly
30. Post
31. Power module
32. Post
33. Stud
34. Lockwasher
35. Screw
36. Lockwasher
37. Screw
38. Lockwasher
39. Screw
40. Lockwasher
41. Screw
42. Rear panel assembly
43. Lockwasher
44. Screw
45. Lockwasher
46. Screw
47. Frame
48. Plate
49. Lockwasher
50. Nut
51. Circuit card AM120

Figure 4-3. Counter, Partial Exploded View

to disassemble posts (8) from the circuit cards.

(h) Remove four screws (13), flat washers (12), and lockwashers (11) holding the circuit cards together. Separate the circuit cards, two posts (8), and two posts (10).

(2) Reassembly.

(a) Assemble circuit cards (9 and 51), two posts (8), and two posts (10).

(b) Secure the circuit cards with four lockwashers (11), flat washers (12), and screws (13).

(c) Secure posts (28) to the assembled circuit cards with two lockwashers (7), flat washers (6) and screws (5).

(d) Position the assembled circuit cards so that the connector on AM120 extends through the opening in the rear panel. Be sure plate (48) is in place.

(e) Secure plate (48) to rear panel assembly (42) with lockwasher (36), screw (37), and nut (50).

(f) Secure the plate and circuit cards to the rear panel assembly with two studs (33), lockwashers (49), and nuts (50).

(g) Secure posts (28) to the frame with two lockwashers (27) and screws (26).

(h) Reconnect the ribbon cables to AM120 and AM121.

(i) Install retainer (22) on the frame and secure with six lockwashers (21) and screws (20).

(j) Install the top and bottom covers.

c. Fan Assembly.

(1) Disassembly.

(a) Remove the top and bottom covers from the counter.

(b) Remove six screws (20, fig. 4-3) and lockwashers (21) securing retainer (22), and remove the retainer.

(c) Unplug the fan wiring harness.

(d) Remove four screws (41) and lockwashers (40) securing fan assembly (2) and spacers (1) to rear panel assembly (42).

(e) Move the assembled fan and spacers forward and out of the top of the counter.

(f) Remove four screws (3) and lockwashers (4) securing two spacers (1) to the fan. Remove the spacers.

(2) Reassembly.

(a) Position two spacers (1) on fan (2) and secure with four lockwashers (4) and screws (3).

(b) Position the assembled fan and spacers on rear panel assembly (42) and secure with four lockwashers (40) and screws (41).

(c) Connect the fan wiring harness.

(d) Install retainer (22) and secure it to the frame with six lockwashers (21) and screws (20).

(e) Install the top and bottom covers.

d. Power Transformer.

(1) Disassembly.

(a) Remove the top and bottom covers from the counter.

(b) Remove six screws (20, fig. 4-3) and lockwashers (21) securing retainer (22) to the frame, and remove the retainer.

(c) Remove four screws (44) and lockwashers (43), from the top and bottom, which secure two corner posts (30) to frame (47).

(d) Remove two screws (46) and lockwashers (45), from the top and bottom, which secure post (32) to frame (47).

(e) Remove four screws (24) and lockwashers (25), from the top and bottom, which secure transformer assembly (29) to frame (47).

(f) Separate the top and bottom frame members to remove two rear corner posts (30) and post (32).

(g) Slide side panel (23) from between the top and bottom frame members.

(h) Remove two nuts (14), lockwashers (15), flat washers (17), and screws (18) which secure POWER switch (19) to circuit card A100 (16).

(i) Remove the switch through the side panel opening.

(j) Cut the cable ties holding the switch wiring harness to the frame.

(k) Remove two nuts (50), lockwashers (49), and studs (33), which secure the connector on circuit card (51) to rear panel assembly (42).

(m) Disconnect the following cables (fig. 4-1):

W22 from A107J1
W23 from A108J1
W24 from A109J6
W25 from A106J6
W26 from A109J3
W27 from A100J8
W28 from A100J1.

(n) Remove rear panel assembly (42, fig. 4-3) from frame (47).

(o) Cut the cable tie securing the inside cover on power module (31). Remove the cover.

(p) Tag and disconnect the wiring from the power module.

(q) Remove rear panel assembly (42).

(r) Unplug the transformer wiring harness from Power Supply A107 (fig. 4-1) and remove transformer assembly (29, fig. 4-3).

(2) Reassembly.

(a) Position transformer assembly (29) between the top and bottom frame members.

(b) Plug the transformer wiring harness into the receptacle on A107 (fig. 4-1).

(c) Connect the tagged leads to power module (31, fig. 4-3).

(d) Install the power module cover and secure with a new cable tie.

(e) Position rear panel assembly (42) in frame (47).

(f) Reconnect the following cables (fig. 4-1):

W22 to A107J1
W23 to A108J1
W24 to A109J6
W25 to A106J6
W26 to A109J3
W27 to A100J8
W28 to A100J1.

(g) Secure the connector on circuit card (51, fig. 4-3) to rear panel assembly (42) with two studs (33), lockwashers (49), and nuts (50).

(h) Position POWER switch (19) on circuit card (16) with the pushbutton extended through the opening in the front panel.

(i) Secure the switch to the circuit card with the screws (18), flat washers (17), lockwashers (15) and nuts (14).

(j) Install the switch wiring harness to the frame with new cable ties.

(k) Slide side panel (23) through the channels between the top and bottom frame members, being careful not to damage the RFI shield braid.

(m) Separate the top and bottom frame members and install post (32) and corner posts (30).

(n) Secure post (32) with two lockwashers (45) and screws (46).

(o) Secure transformer assembly (29) to the frame with four screws (24) and lockwashers (25).

(p) Secure two corner posts (30) to the frame with four screws (44) and lockwashers (43).

(q) Install retainer (22) and secure with six lockwashers (21) and screws (20).

(r) Install the top and bottom covers.

## 4-8. Adjustments.

a. Display Brightness. Relative brightness of the LED displays may be adjusted for the work area conditions encountered. To adjust the brightness, remove the top cover of the counter and adjust resistor A102R35 on Count Chain Control A102 (fig. 4-4). Turning A102R35 clockwise increases the display brightness and counterclockwise decreases the brightness.

b. Power Supply Voltages.

(1) Test, Measurement, and Diagnostic Equipment Required. TMDE (or equivalents) required for power supply adjustments are:

(a) Oscilloscope OS-261/U

(b) Multimeter, Digital AN/USM-451

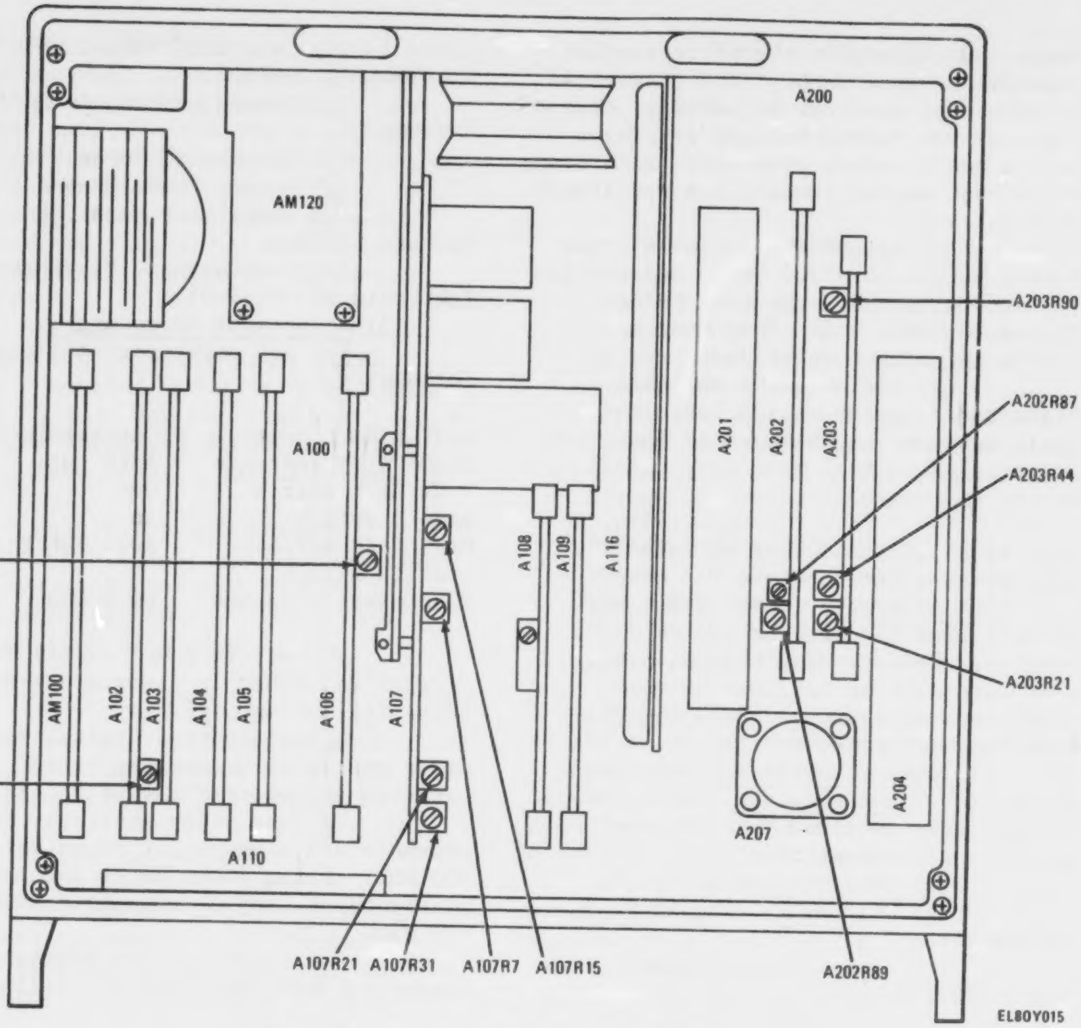

A200
AM120
A203R90
A202R87
A203R44
A100
A106R60
A201
A202
A203
A108
A109
A116
A203R21
AM100
A102
A103
A104
A105
A106
A107
A102R35
A204
A207
A110
A107R21
A107R31
A107R7
A107R15
A202R89
EL80Y015

Figure 4-4. Adjustment Locations

(c) Transformer, Variable, Staco 3PN501V

(2) Adjustment Procedure.

(a) Connect variable transformer to 115 Vac power line and adjust for an output of 115 ± 1 Vac (114 to 116 Vac).

(b) Connect counter power able to variable transformer. Apply ower to counter by pushing POWER ushbutton on front panel. Allow 20 inutes of warm-up time to stabilize ounter components.

(c) Remove top cover and cir uit card retainer.

NOTE

In the following procedures, do not disconnect cable W18 from A100J3 (fig. 4-2). Connect test equipment to A100J3, as specified, by inserting test leads into mating connector of W18.

(d) Connect negative lead of digital multimeter and ground lead of oscilloscope to pin 12 of A100J3.

(e) Connect positive lead of digital multimeter and oscilloscope probe to each test point listed in table 4-3 and adjust the corresponding control on Power Supply A107 (fig. 4-4) to obtain the correct dc voltage. The peak-to-peak ripple voltage displayed on the oscilloscope at each test point should not exceed the maximum specified in table 4-3.

(f) Reduce the variable transformer output to 103.5 Vac. Measure the voltages at each of the test points listed in table 4-3. They must be within the ranges specified.

(g) Increase the variable transformer output to 126.5 Vac and again measure the voltages at each test point to be certain that they remain within tolerance.

(h) Turn off counter, disconnect test equipment, and reinstall circuit card retainer and top cover.

c. Gate Accuracy. This adjustment affects Band A operation and is required whenever High Frequency Circuit Card A106 is replaced or when adjustment is indicated as a troubleshooting corrective action.

(1) Test, Measurement, and Diagnostic Equipment Required. TMDE (or equivalents) required for the gate accuracy adjustment are:

(a) Oscilloscope OS-261/U.

(b) Multimeter, Digital AN/USM-451.

(c) Transformer, Variable, Staco 3PN501V.

(d) Generator Subassembly MX-8364A(P)/USM-308.

(e) Generator Plug In PL-1242/USM-308(V).

(f) Generator, Pulse SG-1105/U.

(g) Meter, Power ME-441/U.

(h) Thermistor Mount, Hewlett-Packard 8478B.

(i) Termination, Feedthrough, Tektronix 011-0049-01.

(2) Adjustment Procedure.

(a) Set counter controls as follows:

| | |
|---|---|
| SAMPLE RATE control | Counterclockwise |
| RESOLUTION switches | Both out |
| 1 ms GATE switch | Out |
| BAND A switch | In |
| MANUAL SELECT/AUTO SWEEP switch | AUTO SWEEP |
| Thumbwheel switches | 00.0 GHz |

(b) Adjust power supply voltages as described in paragraph 4-8b(2), steps (a) through (g).

(c) Disconnect digital voltmeter and oscilloscope, and reset variable transformer output to 115 Vac.

(d) Set sweep generator subassembly and plug-in for cw output at 950 MHz. Using power meter and thermistor mount, adjust cw output level to -10 dBm.

(e) Connect pulse generator output to vertical input of oscilloscope

Table 4-3. Power Supply Voltages and Adjustments

| Test point on A100J3 | DC voltage | Adjustment control | Max. ripple (mV pk-pk) |
|---|---|---|---|
| Pin 9 | +5 V ± 10 mV<br>(+4.990 to +5.010 V) | A107R15 | 10 |
| Pin 11 | +12 V ± 10 mV<br>(+11.990 to +12.010 V) | A107R7 | 12 |
| Pin 8 | -12 V ± 10 mV<br>(-11.990 to -12.010 V) | A107R21 | 12 |
| Pin 10 | -5.2 V ± 10 mV<br>(-5.190 to -5.210 V) | A107R31 | 5 |

through 50 ohm feedthrough termination; termination must be attached directly to oscilloscope input connector. Set up pulse generator for 100 nanosecond pulse width, 50 kHz repetition rate, and -1 volt output level (fig. 4-5).

(f) Connect output of sweep generator and plug-in to BAND A connector on counter. Record cw frequency displayed.

(g) Connect pulse generator output to counter rear-panel INPUT INHIBIT connector. Adjust SAMPLE RATE control so that you can read and record 10 or more displayed frequency readings of the pulsed input. Calculate average of readings.

(h) If average frequency obtained in step (g) is within 1.42 MHz of cw frequency measured in step (f), proceed directly to step (k). Otherwise, continue with step (i).

NOTE

Example: If cw frequency measured in step (f) was 950.00 MHz, averaged frequency obtained in step (g) should be between 948.58 and 951.42 MHz.

(i) Adjust resistor A106R60 (fig. 4-4) to minimize differences between averaged pulse frequency and cw frequency recorded in step (f).

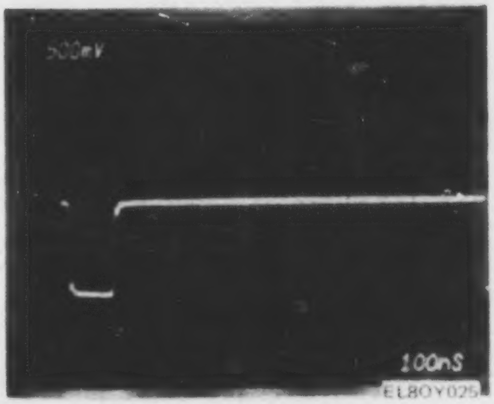


Figure 4-5. Pulse Generator Output

(j) Repeat step (g) to be sure that average of pulsed frequencies is within 1.42 MHz of cw frequency.

(k) Turn off counter, disconnect test equipment, and reinstall circuit card retainer and top cover.

NOTE

The adjustments which follow affect Band B operation and must be performed in the sequence presented, since some adjustments are dependent upon previous ones. The comb level must be set in accordance with paragraph 4-8g after any adjustment is made.

Before making any adjustments, check, and if necessary, adjust the power supply voltages as described in paragraph 4-8b(2), steps (a) through (e).

d. 40 kHz Clock. Adjustment of the 40 kHz clock is required whenever YIG Comb Generator A207 or Converter Sequencer A203 is replaced, or when adjustment is indicated as a troubleshooting corrective action.

(1) Test, Measurement, and Diagnostic Equipment Required. TMDE (or equivalents) required for the 40 kHz clock adjustments are:

(a) Oscilloscope OS-261/U.

(b) Extender, Card, EIP 2020041.

(2) Adjustment Procedure.

(a) Set counter controls as follows:

| | |
|---|---|
| BAND B switch | In |
| MANUAL SELECT/AUTO SWEEP switch | MANUAL SELECT |
| Thumbwheel switches | 01.0 GHz |

(b) Use card extender to elevate YIG Control A202.

(c) Connect jumper between A202TP1 and A202TP3 (fig. 4-6).

(d) Connect jumper between A202TP5 and A202TP9 (ground).

(e) Connect oscilloscope channel 1 to pin 9 of A202U1. Set to 5 V/div.

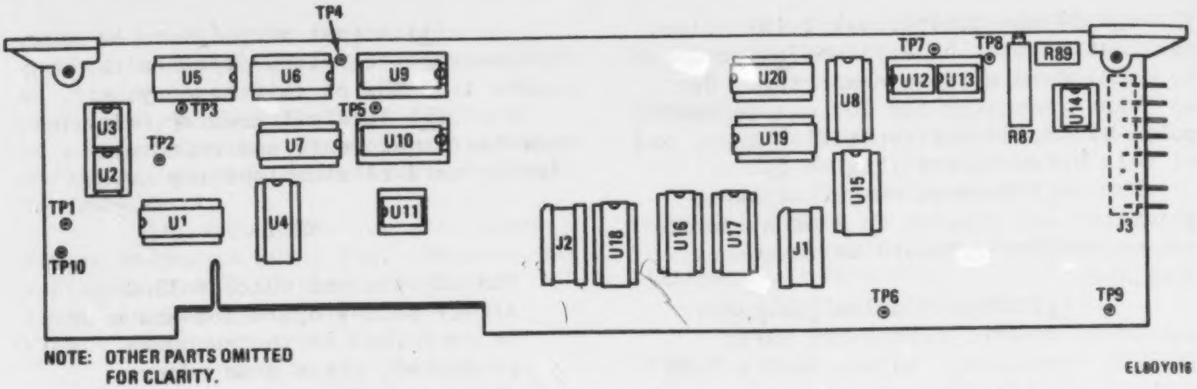

TP4
U5
U6
U9
TP3
TP5
U7
U10
U3
U2
TP2
TP1
U1
U4
U11
TP10
U20
U8
U19
U15
TP7
TP8
U12
U13
R89
R87
U14
J3
J2
U18
U16
U17
J1
TP6
TP9
NOTE: OTHER PARTS OMITTED FOR CLARITY.
EL8OY016

Figure 4-6. YIG Control A202, Adjustment and Test Point Locations

(f) Connect oscilloscope channel 2 to pin 4 of A202U1. Set to 2 V/div.

(g) Apply power to counter.

(h) Adjust resistor A202R89 for symmetrical waveform as shown in channel 1 (upper) trace of fig. 4-7. All pulses in the train should be of equal duration. The channel 1 (upper) trace is the detected modulation pulse and the 20 kHz reference is the channel 2 (lower) trace.

NOTE

> The leading and trailing edges of the 20 kHz reference should be in the center of the detected modulation pulse. If they are not, replace Converter Sequencer A203 and repeat step (h).
>
> Slope and offset adjustments can be made without any changes in the existing test set-up, and are normally accomplished after the 40 kHz clock adjustment. If the 40 kHz clock adjustments bring the counter into normal operation, complete the procedure by disconnecting the two jumpers from test points installed in steps (c) and (d), remove the card extender, and reinstall A202 in the counter.

e. Slope and Offset. The slope and offset adjustment is required whenever YIG Comb Generator A207, Converter Sequencer A203, or YIG Control A202 is replaced, or when adjustment is indicated as a troubleshooting corrective action.

(1) Test, Measurement, and Diagnostic Equipment Required. TMDE (or equivalents) required for the slope and offset adjustment are:

(a) Oscilloscope OS-261/U.

(b) Extender, Card, EIP 2020041.

(2) Adjustment Procedure.

(a) Perform 40 kHz clock adjustment, paragraph 4-8d(2).

(b) Without removing jumpers or oscilloscope leads from A202, change

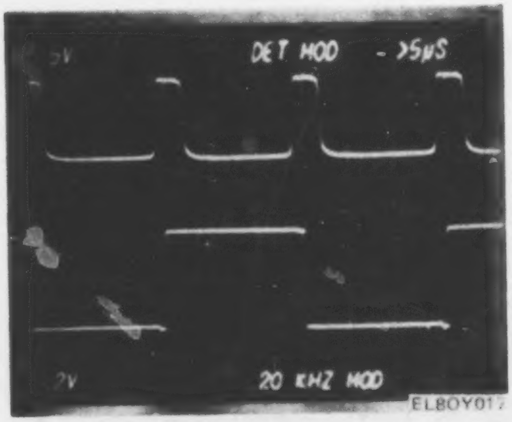

2V
DET MOD - >5µS
2V
20 KHZ MOD
EL8OY017

Figure 4-7. Detected Modulation and 20 kHz Reference Pulse Timing

counter front-panel thumbwheel switch setting in 1 GHz steps from 01.0 through 18.0 GHz and, at each setting, adjust resistor A202R87 (fig. 4-4) for symmetrical waveform (fig. 4-7).

(c) Repeat steps (a) and (b) as necessary to obtain symmetry on the 18 increments from 1 GHz through 18 GHz.

NOTE

Adjustment of A202R87 may affect the previous 40 kHz adjustments. Therefore, this interaction must be compensated for by readjustment of A202R89 for best possible compromise. It may be necessary to go back and forth between the slope and offset adjustment (A202R87) and the 40 kHz clock adjustment (A202R89) to obtain the best possible result.

(d) Disconnect oscilloscope probes.

(e) Disconnect test point jumpers.

(f) Remove card extender and reinstall A202 in counter.

f. Attenuator Driver. Attenuator driver adjustments are required whenever Converter Sequencer A203 or Limiter/Attenuator A206 is replaced, when it is known that the Band B input vswr is too high, or when adjustment is indicated as a troubleshooting corrective action.

(1) Test, Measurement, and Diagnostic Equipment Required. TMDE (or equivalents) required for the attenuator driver adjustments are:

(a) Oscilloscope OS-261/U.

(b) Generator Subassembly MX-8364A(P)/USM-308.

(c) Generator, Sweep, Plug In PL-1304/USM-308(V).

(d) Generator, Sweep, Plug In PL-1242/USM-308(V).

(e) Meter, Power ME-441/U.

(f) Thermistor Mount, Hewlett-Packard 8478B.

(g) Attenuator, Coaxial, Fixed, Hewlett-Packard 8491B-003.

(h) Crystal Detector, Hewlett-Packard 423A.

(i) Directional Coupler, Hewlett-Packard 779D.

(j) Extender, Card, EIP 2020041.

(2) Adjustment Procedure.

(a) Set generator subassembly and plug-in PL-1304/USM-308(V) for cw output at 10 GHz. Using power meter and thermistor mount, adjust cw output level to +7 dBm.

(b) Set counter controls as follows:

| | |
|---|---|
| BAND B switch | In |
| MANUAL SELECT/AUTO SWEEP switch | AUTO SWEEP |
| Thumbwheel switches | 00.0 GHz |

(c) Use card extender to elevate Converter Sequencer A203.

(d) Connect jumper between A203TP16 and A203TP21 (fig. 4-8).

(e) Carefully set up equipment as shown in fig. 4-9. Set oscilloscope for maximum vertical sensitivity, dc coupled.

(f) Apply power to counter.

(g) Adjust A203R44 (fig. 4-8) for maximum return loss, as evidenced by minimum dc level displayed on oscilloscope. A typical oscilloscope display is shown in fig 4-10.

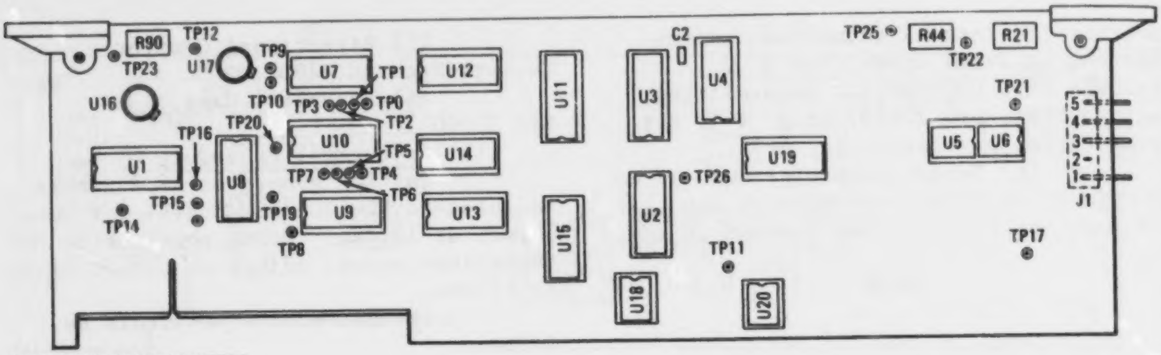
NOTE

As A203R44 is rotated from full counterclockwise to full clockwise position, the dc level displayed on the oscilloscope will go from a maximum through a minimum, and then to a maximum again. The correct adjustment for maximum return loss (minimum reflected signal) corresponds to the minimum dc level.

(h) Remove jumper installed in step (d).

NOTE

If the preceding adjustment was made because A203 or A206 was replaced, omit steps (i) and (j) which follow, and continue with the procedures in paragraph 4-8f(3).


R90
TP12
TP23
U17
TP9
U7
TP1
U12
C2
U4
TP25
R44
TP22
R21
U16
TP10
TP3
TP0
U11
U3
TP21
TP20
TP2
TP16
U10
TP5
U14
U19
U5
U6
U1
U8
TP7
TP4
TP26
5
4
3
2
1
J1
TP15
TP6
TP19
U9
U13
U2
TP14
TP8
U15
TP11
TP17
U18
U20

NOTE: OTHER PARTS OMITTED FOR CLARITY.

EL80Y018

Figure 4-8. Converter Sequencer A203, Adjustment and Test Point Locations

(i) Turn off counter and disconnect test equipment.

(j) Remove card extender and reinstall A203 in counter.

(3) Attenuator Control Test. This test is required only if A203 or A206 has been replaced.

(a) Temporarily connect a 0.47 µf capacitor across A203C2 (fig. 4-8).

(b) Connect oscilloscope channel 1 10X probe to pin 1 of A203J1 (fig. 4-8) to display $I_{series}$, and channel 2 10X probe to A203TP17 to display attenuator control ramp.

(c) Disconnect cable W8 (fig. 4-1) from A204J4 and ground center conductor of cable.

(d) Connect jumper between A203TP14 and A203TP16 (fig. 4-8).

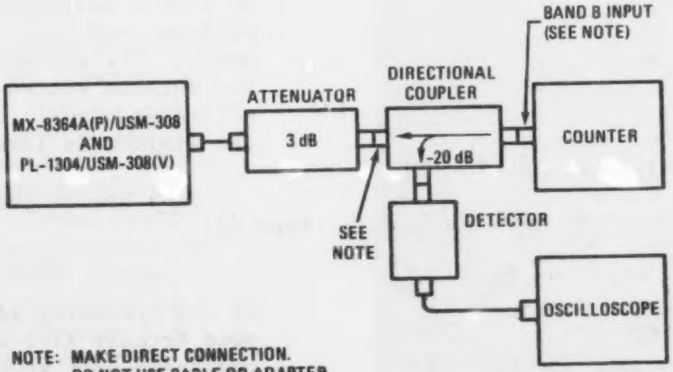
(e) As shown in fig. 4-11, $I_{series}$ (upper trace) should not change during first one to three steps of attenuator control ramp (lower trace). If $I_{series}$ changes, replace A203.

NOTE

If A203 is replaced, repeat steps (a) through (e).

(f) Remove jumper between A203TP14 and A203TP16, remove capacitor connected across A203C2, and reconnect cable W8 to A204J4.

(g) Set generator subassembly and plug-in PL-1242/USM-308(V) for cw output at 1.4 GHz. Using power meter and thermistor mount, adjust cw output level to +5 dBm.


BAND B INPUT
(SEE NOTE)
DIRECTIONAL
COUPLER
ATTENUATOR
MX-8364A(P)/USM-308
AND
PL-1304/USM-308(V)
3 dB
-20 dB
COUNTER
DETECTOR
SEE
NOTE
OSCILLOSCOPE

NOTE: MAKE DIRECT CONNECTION. DO NOT USE CABLE OR ADAPTER AT THIS POINT.

EL80Y019

Figure 4-9. Return Loss Measurement Setup

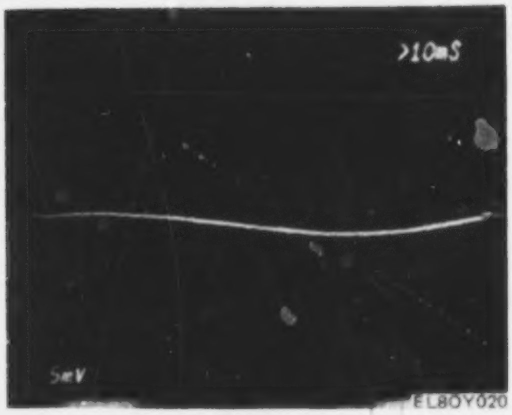


Figure 4-10. Return Loss Measurement Waveform

(h) Connect output of generator subassembly and plug-in to counter BAND B input.

(i) Adjust A203R21 (fig. 4-4) until REDUCE SIGNAL indicator lights.

(j) Press RESET switch and readjust A203R21 as necessary.

(k) Turn off counter and disconnect test equipment.

(m) Remove card extender and reinstall A203 in counter.

g. Comb Leveling. The comb leveling adjustment is required if any of the adjustments covered in paragraphs 4-8d through f have been made.

(1) Test, Measurement, and Diagnostic Equipment Required. TMDE (or equivalents) required for comb leveling are:

(a) Oscilloscope OS-261/U.

(b) Extender, Card, EIP 2020041.

(2) Adjustment Procedure.

(a) Set counter controls as follows:

| | |
|---|---|
| BAND B switch | In |
| MANUAL SELECT/AUTO SWEEP switch | AUTO SWEEP |
| Thumbwheel switches | 00.0 GHz |

(b) Use card extender to elevate Converter Sequencer A203.

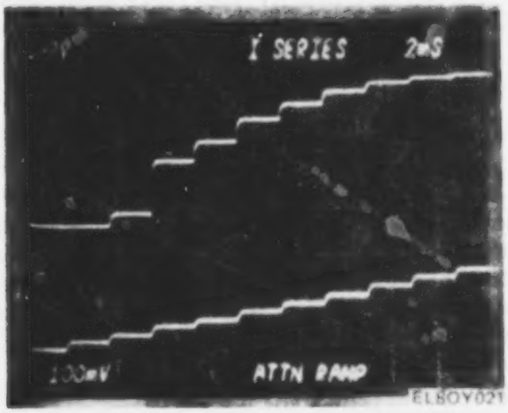


Figure 4-11. Typical Attenuator Control Ramp Offset

(c) Connect A203TP14, A203TP15, and A203TP16 (fig. 4-8) together.

(d) Connect oscilloscope 10X probe to A203TP12 and connect external trigger input to A203TP20.

(e) Apply power to counter.

(f) Adjust A203R90 to level comb line displayed on oscilloscope to nominal 2 volt amplitude, as shown in fig. 4-12.

(g) Turn off counter and disconnect oscilloscope.

(h) Remove jumpers from test points on A203.

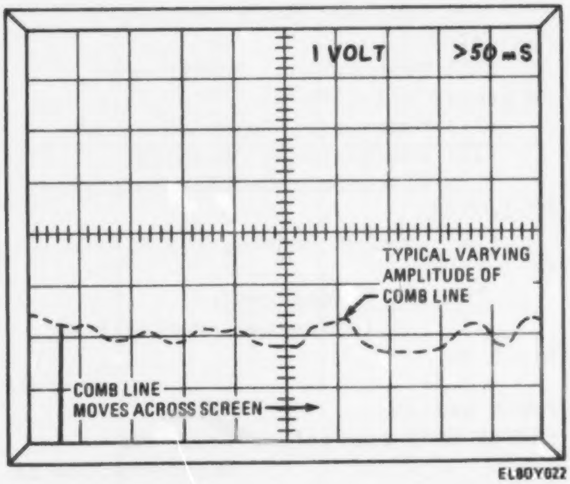

1 VOLT
>50mS
TYPICAL VARYING AMPLITUDE OF COMB LINE
COMB LINE MOVES ACROSS SCREEN
EL8OY022

Figure 4-12. Comb Line

(i) Remove card extender and reinstall A203 in counter.

(j) Reinstall circuit card retainer and top cover.

### 4-9. Performance Test.

a. Purpose. The performance test described in this section of the manual is used to verify that the counter meets its established specifications over the entire frequency range, with both pulsed and cw inputs. The counter should be tested in accordance with these procedures after replacement of any part or assembly.

b. Test, Measurement and Diagnostic Equipment Required. TMDE (or equivalent) required for the performance test are:

(1) Transformer, Variable, Staco 3PN501V.

(2) Meter, Power ME-441/U.

(3) Thermistor Mount, Hewlett-Packard 8478B.

(4) Generator Subassembly MX-8364A(P)/USM-308.

(5) Generator Plug In PL-1240A/USM-308(V).

(6) Generator Plug In PL-1242/USM-308(V).

(7) Generator, Sweep, Plug In PL-1304/USM-308(V).

(8) Oscillator, Sweep, Plug In, Hewlett-Packard 8695A.

(9) Adapter, Hewlett-Packard P281(*)-013.

(10) Termination, Feedthrough, Tektronix 011-0049-01.

(11) Generator, Pulse SG-1105/U.

(12) Oscilloscope OS-261/U.

(13) Electronic Counter Mainframe TD-1209/U.

(14) Counter Module, Electronic TD-1211/U.

c. Initial Procedures.

(1) Set front-panel controls as follows:

| | |
|---|---|
| POWER switch | Off |
| SAMPLE RATE control | Full counterclockwise |
| RESOLUTION switches | Both out |
| 1 ms GATE switch | Out |
| BAND B switch | In |
| MANUAL SELECT/AUTO SWEEP switch | AUTO SWEEP |
| Thumbwheel switches | 00.0 GHz |

(2) Set rear-panel controls as follows:

| | |
|---|---|
| MIN. PRF switch | 50 Hz |
| STORAGE switch | ON |
| GPIB IEEE STD 488/1975 ADDRESS SWITCH | 1 1 0 0 0 0 0 |

NOTE

See fig. 2-8 for explanation of ADDRESS SWITCH positions.

(3) Connect variable transformer to 115 Vac power line and adjust for an output of 115 ± 1 Vac (114 to 116 Vac).

(4) Connect counter power cable to variable transformer. Apply power to counter by pushing POWER switch on. Allow 20 minutes of warm-up time to stabilize counter components.

(5) Check for the following:

(a) Fan is blowing air out of rear panel.

(b) Display shows all zeros.

(c) REDUCE SIGNAL indicator is not lighted.

d. Self-test.

(1) Press TEST DISPLAY switch. Display should indicate 88 888.88 while switch is held in. Release switch.

(2) Press TEST 200 MHz switch. Display should indicate 200.00, with two leading zeros blanked, while switch is held in. Release switch.

(3) Press right RESOLUTION switch and again hold TEST 200 MHz switch in. Display should indicate 200.0, with two leading zeros blanked. Release switch.

(4) While holding TEST 200 MHz switch in, vary variable transformer output from 103.5 to 126.5 Vac. Display must continue to show 200.00 over entire line voltage range.

(5) Release TEST 200 MHz switch and reset variable transformer output to 115 ± 1 Vac.

CAUTION

Throughout the procedures which follow, instructions are given to set various signal sources to specific output levels. In each case, this must be done by measuring the output of the signal source, before connecting it to the counter, using a thermistor mount and rf power meter.

If the signal source is in a sweep mode, the sweep rate must be set at a slow speed to allow monitoring the output power over the sweep range. In no case should the output be allowed to exceed the level specified for each test step.

e. Band B Response.

(1) Set up generator subassembly and plug-in PL-1242/USM-308(V) for -10 dBm cw output at 925 MHz.

(2) Connect generator and plug-in to BAND B input connector. Counter should indicate input frequency of 925 MHz.

(3) Rotate SAMPLE RATE control from full counterclockwise to full clockwise positions, without actuating HOLD switch, and observe LED indicators. LEVEL and LOCK indicators should be lighted continuously; GATE indicator should flash rapidly when SAMPLE RATE control is near counterclockwise extreme, and slowly as control approaches clockwise limit.

(4) Rotate SAMPLE RATE control fully clockwise until HOLD switch actuates. Display should hold last reading. Change generator frequency; counter display should not change.

(5) Push RESET pushbutton and release. Display should now change to new input frequency. Disconnect generator and plug-in from counter.

(6) Turn SAMPLE RATE control to mid-point and push 1 ms GATE switch in.

(7) Adjust generator and plug-in to sweep from 0.925 to 2 GHz at low power level of -10 dBm, as specified in table 4-4. Reconnect plug-in to counter BAND B input connector and set sweep time to permit counter to track swept frequency. Counter should display correct frequency, without dropping out, over entire swept frequency range. REDUCE SIGNAL indicator should not light during any portion of sweep.

(8) Disconnect plug-in from counter and change output to high level of +10 dBm. Reconnect to BAND B connector. Counter should again display correct frequency, without dropping out, over entire swept frequency range.

Table 4-4. Band B Response Tests

| Sweep frequency range (GHz) | Plug-in | Low power level (dBm) | High power level (dBm) |
|---|---|---|---|
| 0.925 - 2 | PL-1242/USM-308(V) | -10 | +10 |
| 2 - 4 | PL-1242/USM-308(V) | -10 | +7 |
| 4 - 8 | PL-1240A/USM-308(V) | -10 | +7 |
| 8 - 10 | PL-1304/USM-308(V) | -10 | +7 |
| 10 - 12.4 | PL-1304/USM-308(V) | -5 | +7 |
| 12.4 - 18 | Hewlett-Packard 8695A with waveguide-to-coax adapter | -5 | +7 |

NOTE

Periodic display hesitation will be noticed.

At an input level approximately +4 to +6 dBm at 1.4 GHz, the REDUCE SIGNAL indicator should be lighted.

(9) Repeat steps (7) and (8) for each frequency range listed in table 4-4, using plug-in specified, at low and high power levels shown in the table.

(10) Disconnect plug-in from counter.

f. Band B Gate Error.

(1) Reset counter front-panel controls as follows:

| | |
|---|---|
| RESOLUTION switches | Both out |
| SAMPLE RATE control | Full counterclockwise |
| 1 ms GATE switch | In |
| MANUAL SELECT/AUTO SWEEP switch | MANUAL SELECT |
| Thumbwheel switches | 01.0 GHz |

(2) Set up generator subassembly and plug-in PL-1242/USM-308(V) for +7 dBm cw output at 1150 MHz.

(3) Connect pulse generator output to vertical input of oscilloscope through 50 ohm feedthrough termination; termination must be attached directly to oscilloscope input connector. Set up pulse generator for 100 nanosecond pulse width, 50 kHz repetition rate, and -1 volt output level (fig. 4-5).

(4) Connect plug-in to BAND B connector on counter. Press RESET switch and record cw frequency displayed.

(5) Connect pulse generator output to counter rear-panel INPUT INHIBIT connector. Adjust SAMPLE RATE control so that you can read and record 10 or more displayed frequency readings of the pulsed input.

(6) Calculate average of readings obtained in step (5). Average should be within 570 kHz of cw frequency measured in step (4).

NOTE

Example: If cw frequency measured in step (4) was 1150.00 MHz, averaged frequency obtained in step (6) should be between 1149.43 and 1150.57 MHz.

(7) Disconnect pulse generator from INPUT INHIBIT connector.

NOTE

The pulse generator must be disconnected from the counter before making measurements at a new frequency to allow for frequency stabilization.

(8) Repeat steps (4) through (7) with +7 dBm cw output from plug-in at the following frequencies: 1200 MHz, 1250 MHz, 1325 MHz, and 1350 MHz.

NOTE

Do not change settings of pulse generator or generator subassembly/plug-in controls at this point.

g. 1 ms Gate.

(1) Set up generator subassembly and plug-in for +7 dBm cw output at 1400 MHz.

(2) Connect plug-in to BAND B connector and pulse generator to INPUT INHIBIT connector.

(3) Connect rear-panel GATE OUTPUT connector to vertical input of oscilloscope through 50 ohm feedthrough termination; termination must be attached directly to oscilloscope input connector.

(4) Press 1 ms GATE time switch on counter.

(5) Verify that a 1 millisecond low-going pulse is displayed, going from 0 Vdc to less than -0.5 Vdc.

(6) Push right-hand RESOLUTION switch.

(7) Verify that a 100 microsecond low-going pulse is displayed, going from 0 Vdc to less than -0.5 Vdc.

NOTE

Do not disconnect test equipment from counter at this point.

h. Signal Threshold.

(1) Move cable from GATE OUTPUT onnector to SIGNAL THRESHOLD OUTPUT onnector.

(2) With counter displaying input requency, signal threshold output dislayed on oscilloscope should be less han -0.5 Vdc.

(3) Remove Band B input signal.

(4) Verify that signal threshold utput signal goes to approximately Vdc.

(5) Disconnect oscilloscope from ounter.

i. Preset Frequencies.

(1) Adjust generator and plug-in or cw output of +7 dBm at 1.0 GHz. econnect plug-in to counter BAND B nput connector.

(2) Set MANUAL SELECT/AUTO SWEEP witch to MANUAL SELECT and set thumbwheel switches to 01.0 GHz, as specified n table 4-5. Display should show all zeros.

(3) Increase input frequency. Counter should start counting at approximately 1.105 GHz (105 MHz above thumbwheel setting).

(4) Continue to increase input frequency. Counter display should drop out at approximately 1.36 GHz (360 MHz above thumbwheel setting).

(5) Lower input frequency to thumbwheel setting of 1.0 GHz. Counter should display all zeros.

(6) Set MANUAL SELECT/AUTO SWEEP switch to AUTO SWEEP. Display should change to some incorrect frequency.

(7) Increase input frequency. Counter should again start counting correctly at approximately 1.105 GHz and continue to count all higher frequencies correctly.

(8) Repeat steps (1) through (7) for all other thumbwheel switch settings listed in table 4-5. Use plug-in, specified in the table, set up to provide +7 dBm cw output at thumbwheel switch frequency. Approximate frequency at which counter should start counting for each switch setting is also shown in the table, along with MANUAL SELECT drop-out frequency.

(9) Disconnect plug-in from counter.

j. Band A Response.

(1) Reset counter front-panel controls as follows:

| | |
|---|---|
| 1 ms GATE switch | Out |
| BAND A switch | In |

Table 4-5. Preset Frequency Tests

| Thumbwheel switch setting (GHz) | Plug-in | Start count frequency (GHz) | MANUAL SELECT drop-out frequency (GHz) |
|---|---|---|---|
| 01.0 | PL-1242/USM-308(V) | 1.105 | 1.36 |
| 01.2 | | 1.305 | 1.56 |
| 01.4 | | 1.505 | 1.76 |
| 01.8 | | 1.905 | 2.16 |
| 02.0 | | 2.105 | 2.36 |
| 04.0 | PL-1240A/USM-308(V) | 4.105 | 4.36 |
| 08.0 | PL-1304/USM-308(V) | 8.105 | 8.36 |
| 10.0 | | 10.105 | 10.36 |

(2) Adjust generator subassembly and plug-in PL-1242/USM-308(V) to sweep from 300 to 950 MHz at output level of -10 dBm.

(3) Connect plug-in to counter BAND A input connector and set sweep time to permit counter to track swept frequency. Counter should display correct frequency, without dropping out, over entire swept frequency range.

(4) Disconnect plug-in from counter and change output level to +10 dBm. Reconnect to BAND A connector. Counter should again display correct frequency, without dropping out, over entire swept frequency.

(5) Disconnect plug-in from counter.

k. Band A Gate Error.

(1) Set up generator subassembly and plug-in PL-1242/USM-308(V) for +7 dBm cw output at 450 MHz.

(2) Connect pulse generator output to vertical input of oscilloscope through 50 ohm feedthrough termination; termination must be attached directly to oscilloscope input connector. Set up pulse generator for 100 nanosecond pulse width, 50 kHz repetition rate, and -1 volt output level (fig. 4-5).

(3) Connect plug-in to BAND A connector on counter. Press RESET switch and record cw frequency displayed.

(4) Connect pulse generator output to counter rear-panel INPUT INHIBIT connector. Adjust SAMPLE RATE control so that you can read and record 10 or more displayed frequency readings of the pulsed input.

(5) Calculate average of readings obtained in step (4). Average should be within 1.42 MHz of cw frequency measured in step (3).

NOTE

Example: If cw frequency measured in step (3) was 450.00 MHz, averaged frequency obtained in step (5) should be between 448.58 and 451.42 MHz.

(6) Disconnect pulse generator from INPUT INHIBIT connector.

NOTE

The pulse generator must be disconnected from the counter before making measurements at a new frequency to allow for frequency stabilization.

(7) Repeat steps (3) through (6) with +7 dBm cw output from plug-in at the following frequencies: 650 MHz, 880 MHz, 925 MHz, and 950 MHz.

(8) Disconnect plug-in from counter.

m. Time Base Frequency. The time base frequency must be measured with the ambient temperature between 0° and 50°C (32° and 122°F).

(1) Connect counter mainframe TD-1209/U with module TD-1211/U to 10 MHz OUTPUT connector on rear panel of counter. Frequency of 10 MHz OUTPUT should be between 9.999980 and 10.000020 MHz.

(2) Reduce output voltage of variable transformer to 103.5 Vac and allow 15 minutes for time base oscillator to stabilize. 10 MHz OUTPUT frequency should be within 1 Hz of frequency measured in step (1).

(3) Repeat step (2) with variable transformer output at 126.5 Vac.

(4) Turn off counter and disconnect all TMDE.

## Section V. PREPARATION FOR STORAGE OR SHIPMENT

### 4-10. Preparation of Equipment.

To prepare the counter for storage or shipment, disconnect the power cable, roll it up, and tie with a strip tie or twine.

### 4-11. Packing Instructions.

a. Support the corners of the counter in styrofoam posts or cushion the counter with cells or pads fabricated of styrofoam or corrugated fiberboard.

b. Place the cushioned unit, together with the power cable and technical manual, within a close-fitting, slotted, corrugated box. Seal the closure with gummed tape and blunt all corners of the box.

c. Place the boxed counter within a moisture-vaporproof barrier, and heat-seal the closure. Then place within a second close-fitting, slotted, corrugated fiberboard box and seal the entire closure with water-resistant tape or adhesive.

d. Overwrap the boxed equipment in waterproof barrier material. Completely seal all joints, seams, and closures with adhesive or other suitable seal equal in moisture resistance to that of the body material.

e. For storage or domestic shipment, place the equipment, packaged as described above, within a close-fitting cardboard shipping carton. Seal the entire closure with water-resistant tape or adhesive and mark the shipping carton in accordance with MIL-STD-129.

WARNING

Prevent personnel injury when applying or removing steel strapping by wearing heavy gloves and protective eyewear. Do not handle packing cartons by the steel strapping.

f. For overseas shipment only, place the equipment, packaged as described in step d, within a nailed wooden box lined inside with a 2-inch thickness of excelsior compacted to 3 pounds per cubic foot. The shipping container should not be lined with a waterproof bag. Strap the shipping container with metal straps and mark in accordance with MIL-STD-129.

Charts Transposed to

End of Volume.

| SEQUENCE | FUNCTION | DURATION |
|---|---|---|
| 0 | Reset - Resets "0" - "9" Detector. | 10 µs |
| 1 | Reset - Counting Chain reset to zero. | 10 µs |
| 2 | Offset Load - Last three DCU's of Count Chain set to any desired number. | 10 µs |
| 3 | Blank | 10 µs |
| 4 | Blank | 10 µs |
| 5 | Blank | 10 µs |
| 6 | Reset Time Base Generator - Resets Time Base Flip-flop and accumulator on A105. | 10 µs |
| 7 | Blank | 10 µs |
| 8 | Signal Gate Enable - Allows Gate Generator (A105) to open the signal gate for the prescribed gate time in response to indication of a measurable input signal to the counter. This is the period when the measurement of input signal frequency actually occurs. | Variable |
| 9 | Blank | 10 µs |
| 10 | Measurement complete - Sets "0" - "9" Detector to show that measurement portion of cycle is complete. | 10 µs |
| 11 | Update Data - Latches associated with each DCU of the counting chain are latched to new DCU data. | 170 µs |
| 12 | End Update Data - Resets update data flip-flops. | 10 µs |
| 13<br>14 | Print - Sends out signal indicating that new measurement data is available. | 20 µs |
| 15 | Display - Starts variable time delay, controlled by SAMPLE RATE control, which separates successive measurement cycles. | Variable |

Table 4-6. CONTROL SEQUENCE

## Display Time Generator

After each measurement is complete, this unit inhibits the Sequence Generator for a time interval determined by the front panel SAMPLE RATE control. In the HOLD position, the inhibit is permanent until a manual or external reset command is applied, or the power is turned off.

The generator includes a variable period one-shot U7B and DCU U8. The one-shot is connected to produce a free running multivibrator during the delay time. Its output drives the DCU, which extends the period of the one-shot by a factor of ten. The only output of the display generator is a sequence inhibit signal. The DCU outputs are combined to inhibit the sequence, in all but the DCU "9" state. This signal is further combined with the sequence "15" and Fast Cycle controls so that inhibit can occur only in sequence "15" with Fast Cycle not applied and with the display generator DCU not in the "9" state. The Hold input keeps the DCU at "0" state, which applies a permanent sequence inhibit in sequence state "15" as long as Fast Cycle is not applied (or the unit reset).

To start the display time, the DCU is set from the previous "9" state to "0" during Sequence "14". At Sequence "15", the display time one-shot is triggered and commences to free run at a rate determined by the SAMPLE RATE control setting (approximately .3 - 30 pulses per second). Unless held reset by a Hold command, the DCU is stepped at this same rate until it reaches state "9". The sequence inhibit is then removed and the sequence continues normally, thus ending the display time.

## Test Mode

The circuits involved in test mode generation are primarily Test Flip-flop U2B. The input command is inverted and drives the flip-flop into the set state. It is held in this state until the input command is removed. Sequence Generator "15" output then resets the flip-flop at the end of the measurement cycle. Outputs of the flip-flop reset the sequence generator at start and finish of TEST, supply TEST commands to the Gate Generator (A105) and the High Frequency (A106) boards, remove the Offset Load command in Band B, and remove the Band A and B control signals to A106. The outputs provided cause the counter to measure an internal 200 MHz test signal as long as the Test Flip-Flop is held set.

## PRF Limit

The PRF Limit circuits receive the input threshold signal from Gate Generator A105. This signal is present whenever the input signal to the counter is above the preset threshold level, and absent when it is below this level. The PRF circuit then produces a continuous output unless gaps in the input exceed about 100 ms, indicating a dropout of the input signal. The PRF Limit Disable input, when active, causes the PRF circuit to produce a permanent high output, despite the disappearance of the input signal.

The PRF circuit includes a one-shot (U6A), triggered by the step which occurs when the input threshold signal disappears. The threshold signal also produces a fast-fall, slow-rising output from inverter U4A with C14, R25, and R26 load. This signal and the one-shot Q output are combined in NAND gate U20D to produce a signal that rises rapidly with appearance of the threshold signal. It does not fall however, unless the threshold signal stays low for more than 100 ms (the time constant of the one-shot.)

# APPENDIX A
# REFERENCES

| | |
|---|---|
| DA Pam 310-1 | Consolidated Index Army Pubs and Forms |
| TB 43-0118 | Field Instructions for Painting and Preserving Electronics Command Equipment Including Camouflage Pattern Painting of Electrical Equipment Shelters |
| TB 43-180 | Calibration Requirements for the Maintenance of Army Materiel. |
| TB 385-4 | Safety Precautions for Maintenance of Electrical/ Electronic Equipment |
| TM 11-6625-2735-14 | Operator's, Organizational, Direct Support, and General Support Maintenance Manual (Including Depot Maintenance) for Oscilloscope OS-261 (NSN 6625-00-127-0079)(NAVELEX 0967-LP-170-1090; TO 33A1-13-498-1) |
| TM 11-6625-2835-14&P | Operator's, Organizational, Direct Support, and General Support Maintenance Manual (Including Repair Parts and Special Tools Lists) for Pulse Generator, SG-1105/U (Hewlett-Packard Model 8013B) (NSN 6625-01-010-3524) |
| TM 11-6625-2953-14 | Operator's, Organizational, Direct Support, and General Support Maintenance Manual; Multimeter, AN/USM-451 (NSN 6625-01-060-6804) |
| TM 38-750 | The Army Maintenance Management System (TAMMS) |
| TM 740-90-1 | Administrative Storage of Equipment |
| TM 750-244-2 | Procedures for Destruction of Electronics Materiel to Prevent Enemy Use (Electronics Command) |

# APPENDIX B
# MAINTENANCE ALLOCATION

## Section I. INTRODUCTION

B-1. General.

This appendix provides a summary of the maintenance operations for Counter, Pulse, Electronic TD-1338(V)1/USM. It authorizes categories of maintenance for specific maintenance functions on repairable items and components and the tools and equipment required to perform each function. This appendix may be used as an aid in planning maintenance operations.

B-2. Maintenance Function.

Maintenance functions will be limited to and defined as follows:

a. Inspect. To determine the serviceability of an item by comparing its physical, mechanical, and/or electrical characteristics with established standards through examination.

b. Test. To verify serviceability and to detect incipient failure by measuring the mechanical or electrical characteristics of an item and comparing those characteristics with prescribed standards.

c. Service. Operations required periodically to keep an item in proper operating condition, i.e., to clean (decontaminate), to preserve, to drain, to paint, or to replenish fuel, lubricants, hydraulic fluids, or compressed air supplies.

d. Adjust. To maintain, within prescribed limits, by bringing into proper or exact position, or by setting the operating charcteristics to the specified parameters.

e. Align. To adjust specified variable elements of an item to bring about optimum or desired performance.

f. Calibrate. To determine and ause corrections to be made or to be adjusted on instruments or test measuring and diagnostic equipments used in precision measurement. Consists of comparisons of two instruments, one of which is a certified standard of known accuracy, to detect and adjust any discrepancy in the accuracy of the instrument being compared.

g. Install. The act of emplacing, seating, or fixing into position an item, part, module (component or assembly) in a manner to allow the proper functioning of the equipment or system.

h. Replace. The act of substituting a serviceable like type part, subassembly, or module (component or assembly) for an unserviceable counterpart.

i. Repair. The application of maintenance services (inspect, test, service, adjust, align, calibrate, replace) or other maintenance actions (welding, grinding, riveting, straightening, facing, remachining, or resurfacing) to restore serviceability to an item by correcting specific damage, fault, malfunction, or failure in a part, subassembly, module (component or assembly), end item, or system.

j. Overhaul. That maintenance effort (service/action) necessary to restore an item to a completely serviceable/operational condition as prescribed by maintenance standards (i.e., DMWR) in appropriate technical publications. Overhaul is normally the highest degree of maintenance performed by the Army. Overhaul does not normally return an item to like new condition.

k. Rebuild. Consists of those services/actions necessary for the restoration of unserviceable equipment to a like new condition in accordance with original manufacturing standards. Rebuild is the highest degree of materiel maintenance applied to Army equipment. The rebuild operation includes the act of returning to zero those age measurements (hours, miles, etc.) considered in classifying Army equipments/components.

B-3. Column Entries.

a. Column 1, Group Number. Column 1 lists group numbers, the purpose of which is to identify components, assemblies, subassemblies, and modules with the next higher assembly.

b. Column 2, Component/Assembly. Column 2 contains the noun names of components, assemblies, subassemblies, and modules for which maintenance is authorized.

c. Column 3, Maintenance Functions. Column 3 lists the functions to be performed on the item listed in column 2. When items are listed without maintenance functions, it is solely for purpose of having the group numbers in the MAC and RPSTL coincide.

d. Column 4, Maintenance Category. Column 4 specifies, by the listing of a "work time" figure in the appropriate subcolumn(s), the lowest level of maintenance authorized to perform the function listed in column 3. This figure represents the active time required to perform that maintenance function at the indicated category of maintenance. If the number or complexity of the tasks within the listed maintenance function vary at different maintenance categories, appropriate "work time" figures will be shown for each category. The number of task-hours specified by the "work time" figure represents the average time required to restore an item (assembly, subassembly, component, module, end item or system) to a serviceable condition under typical field operating conditions. This time includes preparation time, troubleshooting time, and quality assurance/quality control time in addition to the time required to perform the specific tasks identified for the maintenance functions authorized in the maintenance allocation chart. Subcolumns of column 4 are as follows:

C - Operator/Crew
O - Organizational
F - Direct Support
H - General Support
D - Depot

e. Column 5, Tools and Equipment. Column 5 specifies by code, those common tool sets (not individual tools) and special tools, test, and support equipment required to perform the designated function.

f. Column 6, Remarks. Column 6 contains an alphabetic code which leads to the remark in section IV, Remarks, which is pertinent to the item opposite the particular code.

B-4. Tool and Test Equipment Requirements (Section III).

a. Tool or Test Equipment Reference Code. The numbers in this column coincide with the numbers used in the tools and equipment column of the MAC. The numbers indicate the applicable tool or test equipment for the maintenance functions.

b. Maintenance Category. The codes in this column indicate the maintenance category allocated the tool or test equipment.

c. Nomenclature. This column lists the noun name and nomenclature of the tools and test equipment required to perform the maintenance functions.

d. National/NATO Stock Number. This column lists the National/NATO stock number of the specific tool or test equipment.

e. Tool Number. This column lists the manufacturer's part number of the tool followed by the Federal Supply Code for manufacturers (5-digit) in parentheses.

B-5. Remarks (Section IV).

a. Reference Code. This code refers to the appropriate item in section II, column 6.

b. Remarks. This column provides the required explanatory information necessary to clarify items appearing in section II.

## Section II. MAINTENANCE ALLOCATION CHART FOR COUNTER, PULSE, ELECTRONIC TD-1338(V) 1/USM

| (1) GROUP NUMBER | (2) COMPONENT ASSEMBLY | (3) MAINTENANCE FUNCTION | (4) MAINTENANCE CATEGORY | | | | | (5) TOOLS AND EQPT | (6) REMARKS |
|---|---|---|---|---|---|---|---|---|---|
| | | | C | O | F | H | D | | |
| 00 | Counter, Pulse, Electronic TD-1338(V)1/USM | Inspect | | 0.1 | | | | | A |
| | | Test | 0.1 | | | | | | B |
| | | Test | | | | 1.0 | | 1,2,3,4,6,7,8,9,11,12,13,14,21,22,25,26 | C |
| | | Test | | | | | 1.0 | 4,8,11,14,16,17,18 | D |
| | | Repair | 0.1 | | | | | | E |
| | | Repair | | | | 0.8 | 0.8 | 1,20 | F |
| | | Calibrate | | | | | 0.5 | 1,12,13,24 | G |
| | | Adjust | | | | 0.1 | | 1 | H |
| | | Adjust | | | | 0.3 | | 1,2,15,21 | I |
| | | Adjust | | | | 0.5 | | 1,2,3,4,8,11,14,15,21,25 | J |
| | | Adjust | | | | 0.3 | | 1,2,23 | K |
| | | Adjust | | | | 0.3 | | 1,2,23 | L |
| | | Adjust | | | | 0.3 | | 1,2,23 | M |
| | | Adjust | | | | 0.5 | | 1,2,4,5,6,8,10,11,14,19,23 | N |
| 01 | Counter, basic | | | | | | | | |
| 02 | Converter | | | | | | | | |

## Section III. TOOL AND TEST EQUIPMENT REQUIREMENTS FOR COUNTER, PULSE, ELECTRONIC TD-1338(V) 1/USM

| TOOL OR TEST EQUIP. REF CODE | MAINTENANCE CATEGORY | NOMENCLATURE | NATIONAL/NATO STOCK NUMBER | TOOL NUMBER |
|---|---|---|---|---|
| 1 | H,D | Tool Kit, Electronic Equipment TK-105/G | 5180-00-610-8177 | |
| 2 | H,D | Oscilloscope OS-261/U | 6625-00-127-0079 | |
| 3 | H,D | Generator, Pulse SG-1105/U | 6625-01-010-3524 | |
| 4 | H,D | Generator Subassembly MX-8364A(P)/USM-308 | 6625-00-442-3470 | |
| 5 | H,D | Coupler, Directional (Hewlett-Packard 779D) | | |
| 6 | H,D | Generator, Sweep, Plug In PL-1304/USM-308(V) | 6625-00-444-2327 | |
| 7 | H,D | Oscillator, Sweep, Plug In (Hewlett-Packard 8695A) | 6625-00-928-0368 | |
| 8 | H,D | Generator Plug In PL-1242/USM-308(V) | 6625-00-251-5212 | |
| 9 | H,D | Generator Plug In PL-1240/USM-308(V) | 6625-00-165-1263 | |
| 10 | H,D | Detector, Crystal (Hewlett-Packard 423A) | | |
| 11 | H,D | Meter, Power ME-441/U | 6625-00-436-4883 | |
| 12 | H,D | Electronic Counter Mainframe TD-1209/U | 6625-00-024-7066 | |
| 13 | H,D | Counter Module, Electronic TD-1211/U | 6625-00-298-9676 | |
| 14 | H,D | Thermistor Mount (Hewlett-Packard 8478B) | | |
| 15 | H,D | Multimeter, Digital AN/USM-451 | 6625-00-168-0585 | |
| 16 | D | Computer, Desktop (Hewlett-Packard 9825A) | | |
| 17 | D | Interface, GPIB (Hewlett-Packard 98034A) | | |
| 18 | D | Cable, GPIB (Hewlett-Packard 10833(*)) | | |
| 19 | H,D | Attenuator, Coaxial, Fixed (Hewlett-Packard 8491B-003) | | |
| 20 | H,D | Tool, IC Extractor (Augat T114-1) | | |
| 21 | H,D | Transformer, Variable (Staco 3PN501V) | | |
| 22 | H,D | Generator, Delay (EIP 400) | | |
| 23 | H,D | Extender, Card (EIP 2020041) | | |
| 24 | H,D | Thermometer, Precision/Scientific, 0-50°C | | |
| 25 | H,D | Termination, Feedthrough (Tektronix 011-0049-01) | | |
| 26 | H,D | Adapter (Hewlett-Packard P281(*)-013) | | |

## Section IV. REMARKS

| REFERENCE CODE | REMARKS |
|---|---|
| A | Visual inspection |
| B | Self-test only |
| C | Test after replacing card or module |
| D | GPIB operational test |
| E | Repair by replacing fuse or power cable |
| F | Repair by replacing card or module |
| G | Reference oscillator calibration |
| H | Display brightness adjustment |
| I | Power supply voltage adjustment |
| J | Gate ramp adjustment |
| K | YIG comb line adjustment |
| L | 40 kHz clock adjustment |
| M | Slope and offset adjustment |
| N | Attenuator driver adjustment |

best copy available

# APPENDIX C
# COMPONENTS OF END ITEM AND BASIC ISSUE ITEMS LISTS

Not applicable

# APPENDIX D
# ADDITIONAL AUTHORIZATION LIST

Not applicable

# APPENDIX E
# EXPENDABLE SUPPLIES AND MATERIALS LIST

Not applicable

## RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS

THEN...JOT DOWN THE DOPE ABOUT IT ON THIS FORM. CAREFULLY TEAR IT OUT, FOLD IT AND DROP IT IN THE MAIL.

## SOMETHING WRONG WITH THIS PUBLICATION?

FROM: (PRINT YOUR UNIT'S COMPLETE ADDRESS
Your mailing address

DATE SENT Date you filled out form

| PUBLICATION NUMBER | PUBLICATION DATE | PUBLICATION TITLE |
|---|---|---|
| TM 11-XXXX-XXXX-XX | Date of TM | Title of TM |

| BE EXACT PIN-POINT WHERE IT IS | | | | IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT: |
|---|---|---|---|---|
| PAGE NO. | PARA-GRAPH | FIGURE NO. | TABLE NO. | |
| 400 | | 183 | | Change illustration. Reason: Tube end shown assembled on wrong side of lever cam. |
| 512 | | 191 | | Figure 191, item 3 has wrong NSN. Supply rejects orders for this item. The NSN shown here is not listed in the AMDF or the MCRL.<br>Please give us the correct NSN and P/N. |

SAMPLE

PRINTED NAME GRADE OR TITLE AND TELEPHONE NUMBER
JOHN SMITH, S. Sgt 201-555-XXXX

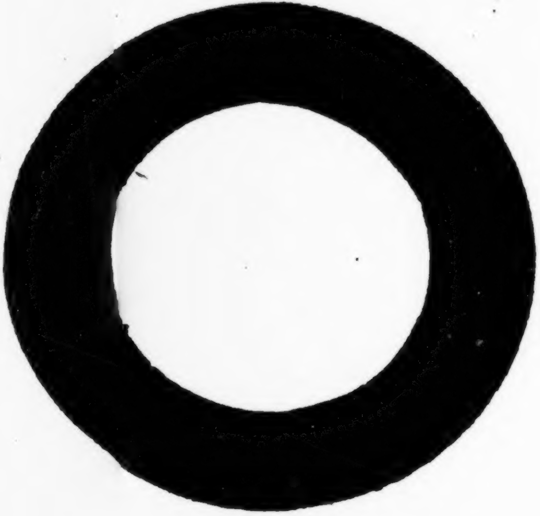
SIGN HERE John Smith

DA FORM 1 JUL 79 2028-2

PREVIOUS EDITIONS ARE OBSOLETE

P.S.--IF YOUR OUTFIT WANTS TO KNOW ABOUT YOUR RECOMMENDATION MAKE A CARBON COPE OF THIS AND GIVE IT TO YOUR HEADQUARTERS.

TEAR ALONG PERFORATED LINE



TEAR ALONG PERFORATED LINE

## RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS

**SOMETHING WRONG** WITH THIS PUBLICATION?

*THEN...JOT DOWN THE DOPE ABOUT IT ON THIS FORM. CAREFULLY TEAR IT OUT, FOLD IT AND DROP IT IN THE MAIL.*

FROM: (PRINT YOUR UNIT'S COMPLETE ADDRESS

DATE SENT

| | | |
|---|---|---|
| PUBLICATION NUMBER<br>TM 11-6625-3031-14 | PUBLICATION DATE<br>6 MAY 83 | PUBLICATION TITLE<br>Counter, Pulse, Electronic<br>TD-1338(V)1/U |

BE EXACT PIN-POINT WHERE IT IS

| PAGE NO. | PARA-GRAPH | FIGURE NO. | TABLE NO. |
|---|---|---|---|
| | | | |

IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:

PRINTED NAME GRADE OR TITLE AND TELEPHONE NUMBER

SIGN HERE

DA FORM 1 JUL 79 2028-2

PREVIOUS EDITIONS ARE OBSOLETE

P.S.--IF YOUR OUTFIT WANTS TO KNOW ABOUT YOUR RECOMMENDATION MAKE A CARBON COPE OF THIS AND GIVE IT TO YOUR HEADQUARTERS.

REVERSE OF DA FORM 2028-2

TEAR ALONG PERFORATED LINE

FILL IN YOUR UNIT'S ADDRESS

FOLD BACK

**DEPARTMENT OF THE ARMY**

____________________________

____________________________

**OFFICIAL BUSINESS**

Commander
US Army Communications-Electronics Command
and Fort Monmouth
ATTN: DRSEL-ME-MP
Fort Monmouth, New Jersey 07703

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS

THEN...JOT DOWN THE DOPE ABOUT IT ON THIS FORM. CAREFULLY TEAR IT OUT, FOLD IT AND DROP IT IN THE MAIL.

**SOMETHING WRONG** WITH THIS PUBLICATION?

FROM: (PRINT YOUR UNIT'S COMPLETE ADDRESS

DATE SENT

| | | |
|---|---|---|
| PUBLICATION NUMBER<br>TM 11-6625-3031-14 | PUBLICATION DATE<br>6 MAY 83 | PUBLICATION TITLE<br>Counter, Pulse, Electronic TD-1338(V)1/U |

BE EXACT PIN-POINT WHERE IT IS

| PAGE NO. | PARA-GRAPH | FIGURE NO. | TABLE NO. | IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT: |
|---|---|---|---|---|
| | | | | |

PRINTED NAME GRADE OR TITLE AND TELEPHONE NUMBER

SIGN HERE

DA FORM 1 JUL 79 2028-2

PREVIOUS EDITIONS ARE OBSOLETE

P.S.--IF YOUR OUTFIT WANTS TO KNOW ABOUT YOUR RECOMMENDATION MAKE A CARBON COPE OF THIS AND GIVE IT TO YOUR HEADQUARTERS.

TEAR ALONG PERFORATED LINE

REVERSE OF DA FORM 2028-2

FILL IN YOUR
UNIT'S ADDRESS

FOLD BACK

TEAR ALONG PERFORATED LINE

DEPARTMENT OF THE ARMY

OFFICIAL BUSINESS

Commander
US Army Communications-Electronics Command
and Fort Monmouth
ATTN: DRSEL-ME-MP
Fort Monmouth, New Jersey 07703

TEAR ALONG PERFORATED LINE

## RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS

**SOMETHING WRONG** WITH THIS PUBLICATION?

THEN...JOT DOWN THE DOPE ABOUT IT ON THIS FORM. CAREFULLY TEAR IT OUT, FOLD IT AND DROP IT IN THE MAIL.

FROM: (PRINT YOUR UNIT'S COMPLETE ADDRESS

DATE SENT

| PUBLICATION NUMBER | PUBLICATION DATE | PUBLICATION TITLE |
|---|---|---|
| TM 11-6625-3031-14 | 6 MAY 83 | Counter, Pulse, Electronic<br>TD-1338(V)1/U |

BE EXACT PIN-POINT WHERE IT IS

| PAGE NO. | PARA-GRAPH | FIGURE NO. | TABLE NO. | IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT: |
|---|---|---|---|---|
| | | | | |

PRINTED NAME GRADE OR TITLE AND TELEPHONE NUMBER

SIGN HERE

DA FORM 1 JUL 79 2028-2

PREVIOUS EDITIONS ARE OBSOLETE

P.S.--IF YOUR OUTFIT WANTS TO KNOW ABOUT YOUR RECOMMENDATION MAKE A CARBON COPE OF THIS AND GIVE IT TO YOUR HEADQUARTERS.

REVERSE OF DA FORM 2028-2

FILL IN YOUR UNIT'S ADDRESS

FOLD BACK

DEPARTMENT OF THE ARMY

____________________________

____________________________

OFFICIAL BUSINESS

Commander
US Army Communications-Electronics Command
and Fort Monmouth
ATTN: DRSEL-ME-MP
Fort Monmouth, New Jersey 07703

TEAR ALONG PERFORATED LINE

By Order of the Secretary of the Army:

E. C. MEYER
*General, United States Army*
*Chief of Staff*

Official:
ROBERT M. JOYCE
*Major General, United States Army*
*The Adjutant General*

DISTRIBUTION:

To be distributed in accordance with Special List.

☆U.S. GOVERNMENT PRINTING OFFICE: 1990 - 261-872/20949

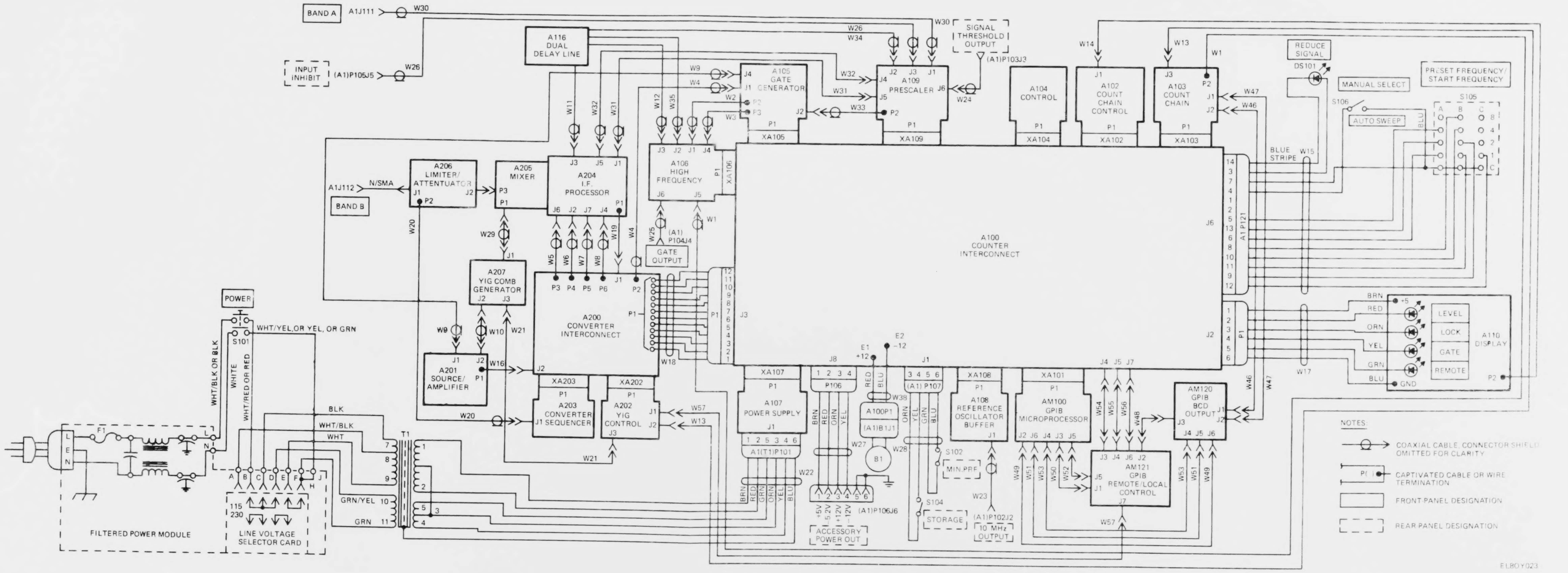
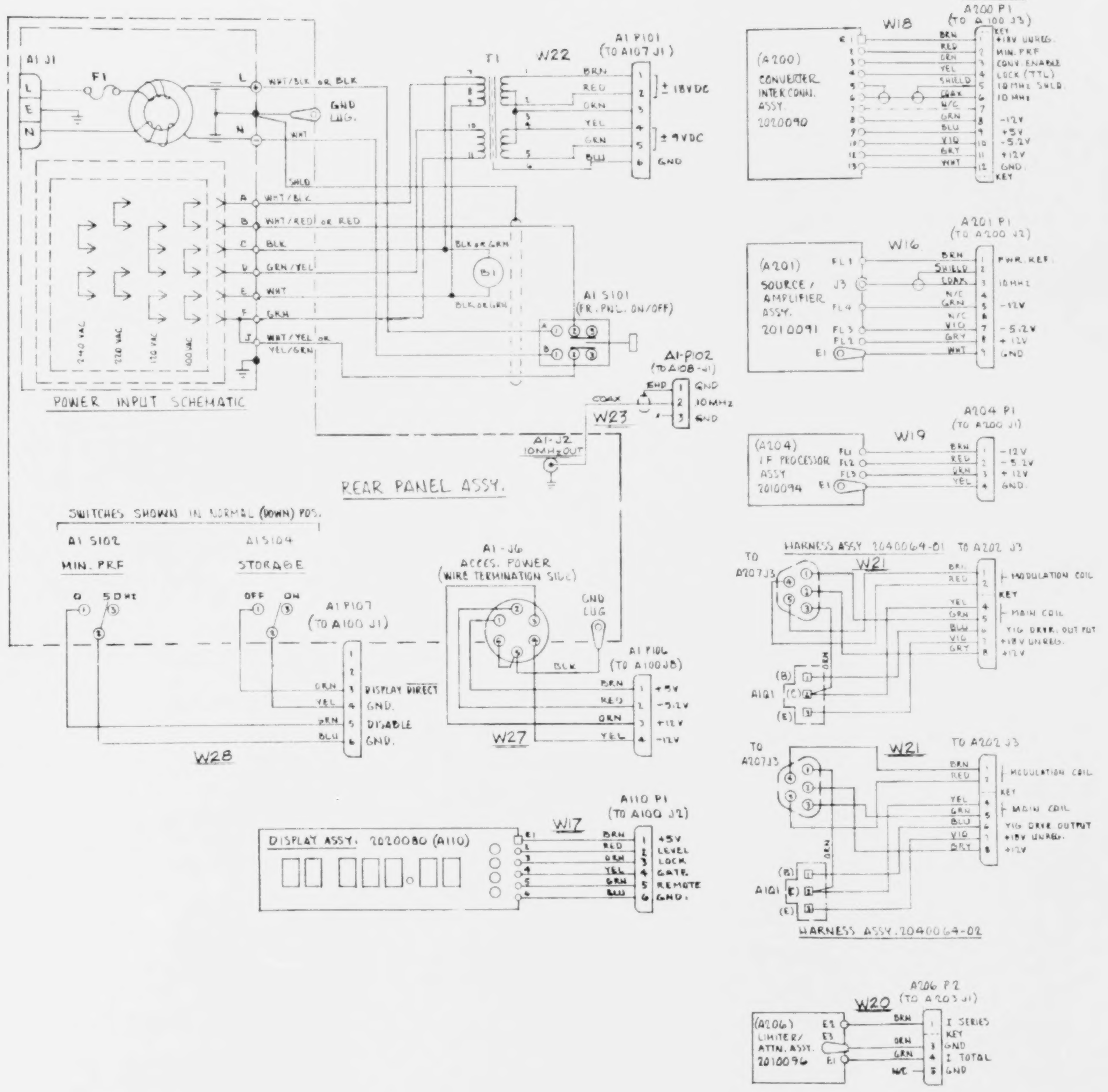

BAND A
A1J111
W30
INPUT INHIBIT
(A1)P105J5
W26
A116 DUAL DELAY LINE
W26
W34
W30
SIGNAL THRESHOLD OUTPUT
(A1)P103J3
A105 GATE GENERATOR
A109 PRESCALER
A104 CONTROL
A102 COUNT CHAIN CONTROL
A103 COUNT CHAIN
REDUCE SIGNAL
DS101
MANUAL SELECT
PRESET FREQUENCY/ START FREQUENCY
S106
AUTO SWEEP
S105
XA105
XA109
XA104
XA102
XA103
BLUE STRIPE
W15
A1J112
N/SMA
BAND B
A206 LIMITER/ ATTENTUATOR
A205 MIXER
A204 I.F. PROCESSOR
A106 HIGH FREQUENCY
XA106
(A1) P104J4
GATE OUTPUT
A100 COUNTER INTERCONNECT
A1P121
A207 YIG COMB GENERATOR
A200 CONVERTER INTERCONNECT
POWER
S101
WHT/YEL,OR YEL, OR GRN
WHT/BLK OR BLK
WHITE
WHT/RED OR RED
A201 SOURCE/ AMPLIFIER
W16
XA203
XA202
A203 CONVERTER J1 SEQUENCER
A202 YIG CONTROL
W20
W21
W57
W13
BLK
WHT/BLK
WHT
T1
GRN/YEL
GRN
115
230
LINE VOLTAGE SELECTOR CARD
FILTERED POWER MODULE
F1
E1 +12
E2 -12
XA107
A107 POWER SUPPLY
A1(T1)P101
BRN RED ORN GRN YEL BLU
W22
J8
P106
A100P1
(A1)B1J1
W38
W27
W28
B1
+5V +5.2V -12V +12V
(A1)P106J6
ACCESSORY POWER OUT
(A1) P107
S102
MIN PRF
S104
STORAGE
XA108
A108 REFERENCE OSCILLATOR BUFFER
W23
(A1)P102J2
10 MHz OUTPUT
XA101
AM100 GPIB MICROPROCESSOR
W54 W55 W56 W48
W49 W51 W53 W50 W52
AM121 GPIB REMOTE/LOCAL CONTROL
AM120 GPIB BCD OUTPUT
W53 W51 W49
W47
W46
W17
BRN
RED
ORN
YEL
GRN
BLU
GND
+5
LEVEL
LOCK
GATE
REMOTE
A110 DISPLAY
P2
NOTES:
COAXIAL CABLE, CONNECTOR SHIELD OMITTED FOR CLARITY
P( )
CAPTIVATED CABLE OR WIRE TERMINATION
FRONT-PANEL DESIGNATION
REAR PANEL DESIGNATION
ELBOY023

Figure FO-1
Counter Interconnection
Schematic Diagram

best copy available


A1 J1
L
E
N
F1
GND LUG.
WHT/BLK OR BLK
WHT
SHLD
A WHT/BLK
B WHT/RED OR RED
C BLK
D GRN/YEL
E WHT
F GRN
J WHT/YEL OR YEL/GRN
240 VAC
220 VAC
120 VAC
100 VAC
POWER INPUT SCHEMATIC
T1
W22
A1 P101 (TO A107 J1)
BRN
RED
ORN
YEL
GRN
BLU
± 18VDC
± 9VDC
GND
B1
BLK OR GRN
A1 S101 (FR. PNL. ON/OFF)
A1-P102 (TO A108-J1)
SHD
COAX
W23
1 GND
2 10MHz
3 GND
A1-J2 10MHz OUT
REAR PANEL ASSY.
SWITCHES SHOWN IN NORMAL (DOWN) POS.
A1 S102
MIN. PRF
0
50Hz
A1 S104
STORAGE
OFF
ON
A1 P107 (TO A100 J1)
ORN 3 DISPLAY DIRECT
YEL 4 GND.
GRN 5 DISABLE
BLU 6 GND.
W28
A1-J6 ACCES. POWER (WIRE TERMINATION SIDE)
GND LUG
BLK
A1 P106 (TO A100 J8)
BRN 1 +5V
RED 2 -5.2V
ORN 3 +12V
YEL 4 -12V
W27
DISPLAY ASSY. 2020080 (A110)
W17
A110 P1 (TO A100 J2)
BRN 1 +5V
RED 2 LEVEL
ORN 3 LOCK
YEL 4 GATE
GRN 5 REMOTE
BLU 6 GND.
(A200) CONVERTER INTERCONN. ASSY. 2020090
W18
A200 P1 (TO A100 J3)
KEY
BRN 1 +18V UNREG.
RED 2 MIN. PRF
ORN 3 CONV. ENABLE
YEL 4 LOCK (TTL)
SHIELD 5 10MHz SHLD.
COAX 6 10MHz
N/C 7
GRN 8 -12V
BLU 9 +5V
VIO 10 -5.2V
GRY 11 +12V
WHT 12 GND
KEY
(A201) SOURCE/AMPLIFIER ASSY. 2010091
FL1
J3
FL4
FL3
FL2
E1
W16
A201 P1 (TO A200 J2)
BRN 1 PWR. REF.
SHIELD 2
COAX 3 10MHz
N/C 4
GRN 5 -12V
N/C 6
VIO 7 -5.2V
GRY 8 +12V
WHT 9 GND
(A204) I F PROCESSOR ASSY 2010094
W19
A204 P1 (TO A200 J1)
BRN 1 -12V
RED 2 -5.2V
GRN 3 +12V
YEL 4 GND.
HARNESS ASSY 2040064-01 TO A202 J3
TO A207J3
W21
BRN 1
RED 2
MODULATION COIL
KEY
YEL 4
GRN 5
MAIN COIL
BLU 6 YIG DRVR. OUTPUT
VIO 7 +18V UNREG.
GRY 8 +12V
ORN
A1Q1
(B)
(C)
(E)
W21
TO A202 J3
HARNESS ASSY. 2040064-02
(A206) LIMITER/ATTN. ASSY. 2010096
E2
E3
E1
W20
A206 P2 (TO A203 J1)
BRN 1 I SERIES
KEY
ORN 3 GND
GRN 4 I TOTAL
N/C 5 GND

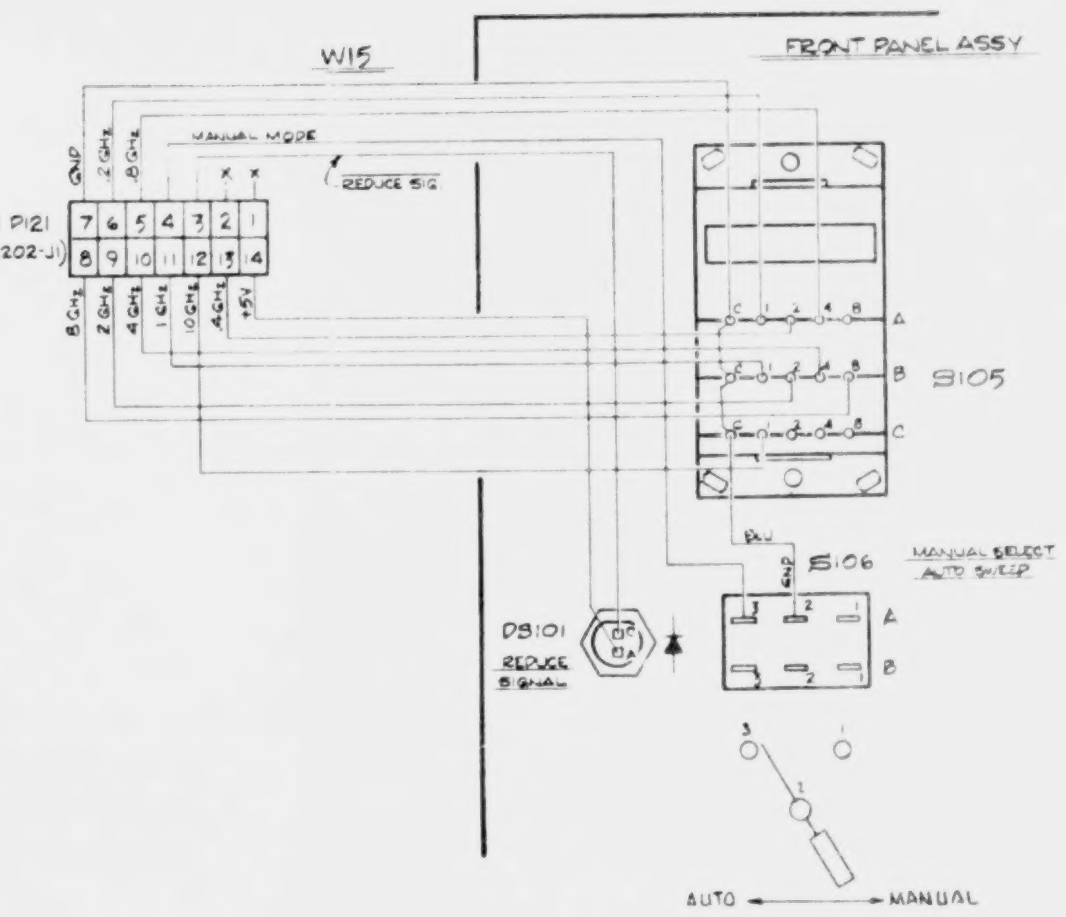
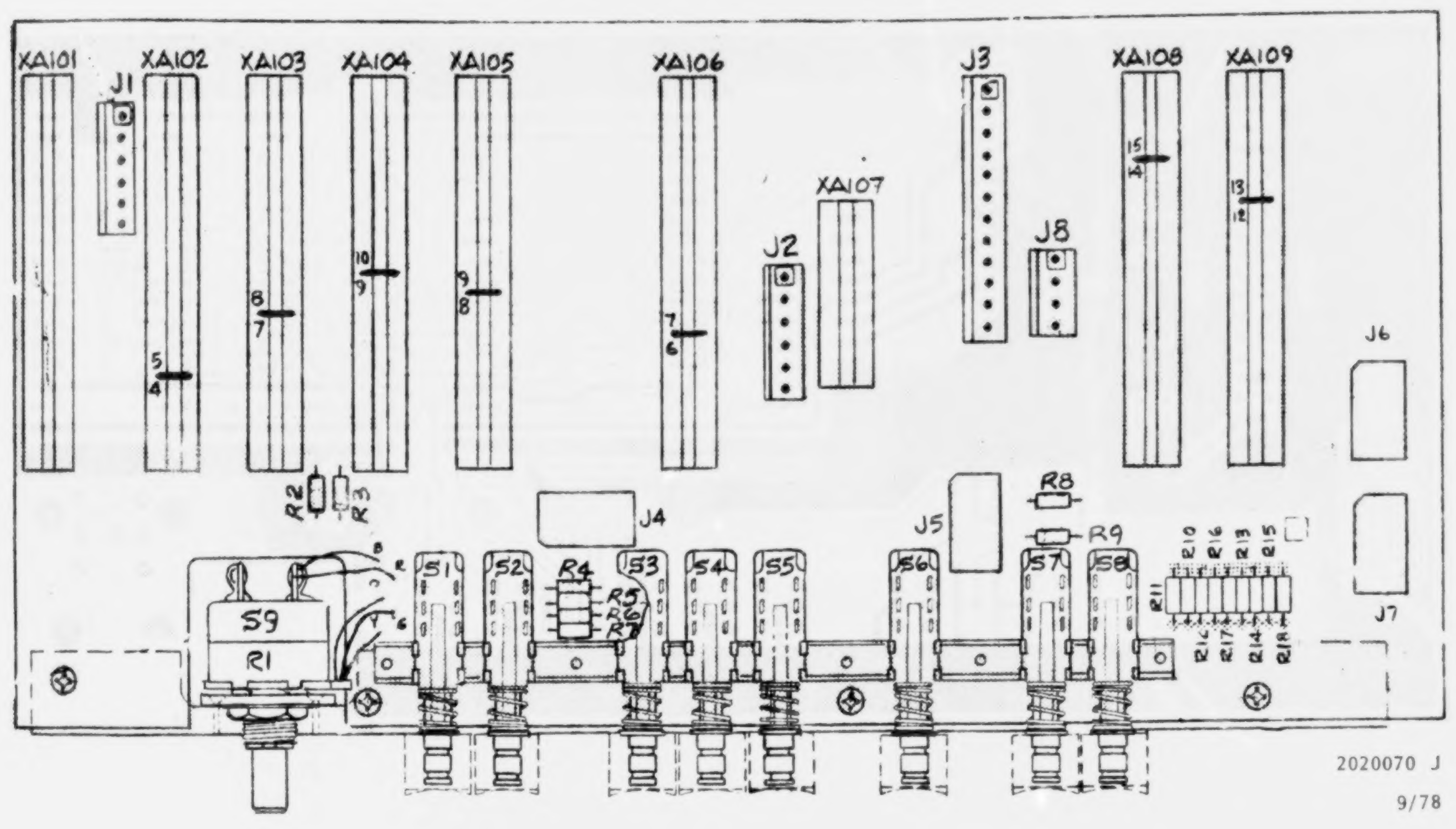

W15
FRONT PANEL ASSY
GND
.2GHz
.8GHz
MANUAL MODE
REDUCE SIG
A1 P121 (TO A202-J1)
8GHz
2GHz
4GHz
1GHz
10GHz
.4GHz
+5V
S105
A
B
C
BLU
GND
S106
MANUAL SELECT
AUTO SWEEP
DS101
REDUCE SIGNAL
AUTO
MANUAL

Figure FO-2
INTERCONNECTION
DIAGRAM
Detailed Technical Schematic


XA101
XA102
XA103
XA104
XA105
XA106
XA107
XA108
XA109
J1
J2
J3
J4
J5
J6
J7
J8
R1
R2
R3
R4
R8
R9
S1
S2
S3
S4
S5
S6
S7
S8
S9
2020070 J
9/78

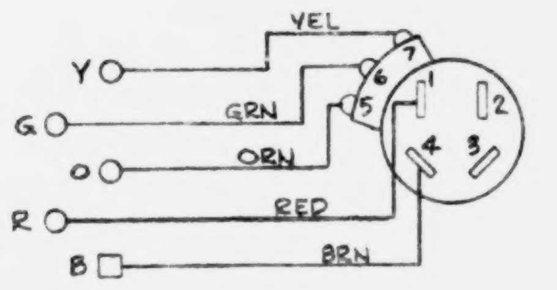

Y
G
O
R
B
YEL
GRN
ORN
RED
BRN
1
2
3
4
5
6
7

Figure FO-3A

COMPONENT LOCATOR
COUNTER INTERCONNECT (A100)

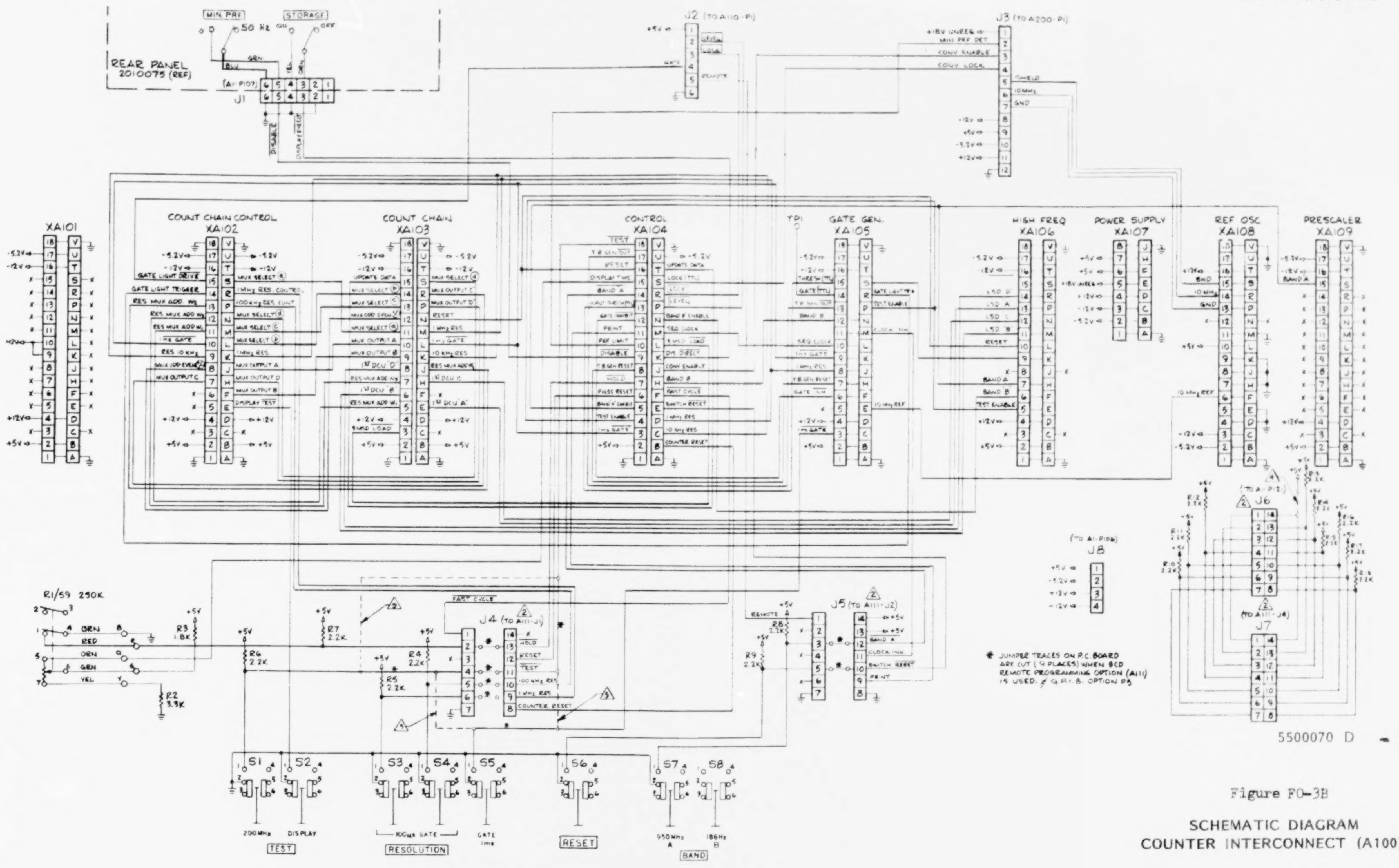
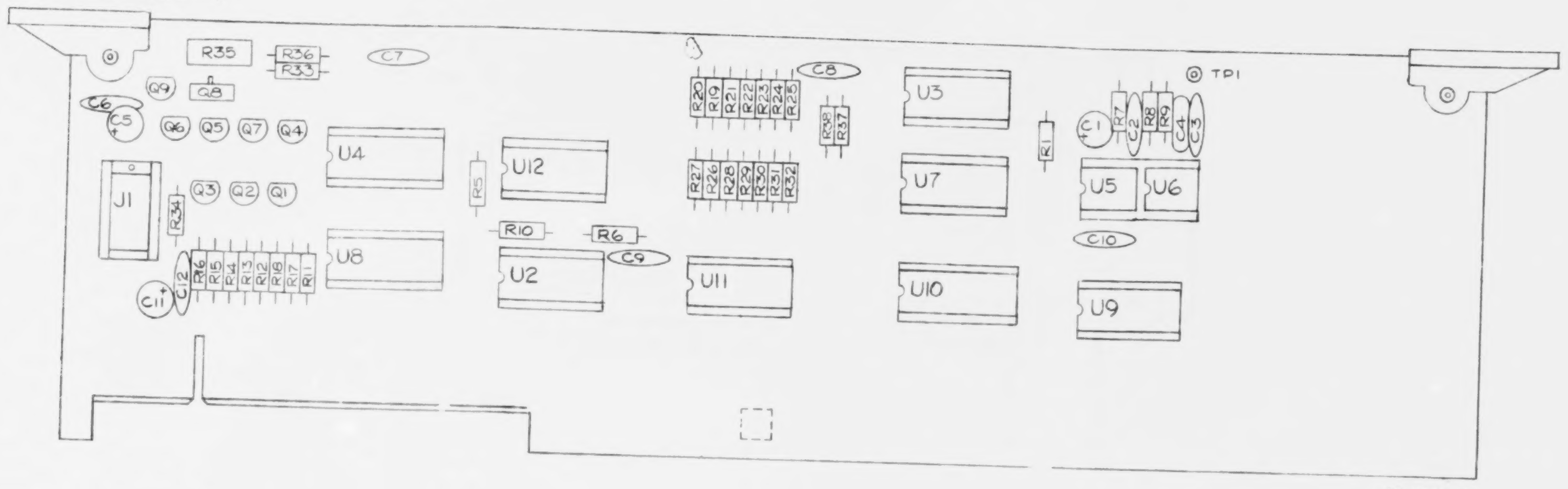

MIN PRF
50 Hz
STORAGE
ON
OFF
REAR PANEL
2010075 (REF)
(A1-P107)
J1
DISABLE
DISPLAY DIRECT
J2 (TO A110-P1)
J3 (TO A200-P1)
SHIELD
10MHz
GND
XA101
COUNT CHAIN CONTROL
XA102
COUNT CHAIN
XA103
CONTROL
XA104
TP1
GATE GEN.
XA105
HIGH FREQ
XA106
POWER SUPPLY
XA107
REF OSC
XA108
PRESCALER
XA109
(TO A1-P12)
J6
J7
(TO A1-P106)
J8
R1/S9 250K
BRN
RED
ORN
GRN
YEL
R2
3.3K
R3
1.8K
R4
2.2K
R5
2.2K
R6
2.2K
R7
2.2K
R8
2.2K
R9
2.2K
FAST CYCLE
J4 (TO A111-J1)
HOLD
RESET
TEST
100 kHz RES
1 MHz RES
COUNTER RESET
J5 (TO A111-J2)
REMOTE
BAND A
CLOCK INH
SWITCH RESET
PRINT
* JUMPER TRACES ON P.C. BOARD ARE CUT (4 PLACES) WHEN BCD REMOTE PROGRAMMING OPTION (A111) IS USED. & G.P.I.B. OPTION P3
S1
S2
S3
S4
S5
S6
S7
S8
200MHz
DISPLAY
TEST
100μs GATE
GATE 1ms
RESOLUTION
RESET
950MHz A
18GHz B
BAND
5500070 D

Figure FO-3B

SCHEMATIC DIAGRAM
COUNTER INTERCONNECT (A100)



## COUNT CHAIN CONTROL (A102)

### General

Count Chain Control A102 controls and processes the flow of information on Count Chain board A103, and drives the front panel visual display. A pulse-stretcher and driver (on A102) also operate the **GATE** indicator on the front panel of the counter.

The clock generator, a ÷16 counter, and a 3-8 line decoder, serve to produce a sequence of eight addresses. These cause the DCU's on A103 to read out their BCD contents, in sequence, back to the data input of A102. The digits of the number representing the frequency measured by the counter are thus read in sequence into A102. The BCD numbers are decoded by U8 to drive the segments of each display digit on Display board A110. The same address generator that selected DCU's on A103, now addresses and drives the proper display digit of A110, so the number of a particular DCU of A103 will be displayed in the proper position. The address drive to certain display digits may be removed (to blank these digits) via the **RESOLUTION** switches.

The gate trigger is applied to a pulse-stretcher on A102. This insures that the gate control signal is of sufficient duration that the **GATE** indicator will produce a visible flash for each measurement cycle of the counter. (Short gates of 100 μs would not otherwise be visible.)

### Display Address Generator (U6, U9-11)

The Address Generator is driven by the clock generated in U6 at a 200 kHz rate. This drives binary counter U9, producing a sequence of sixteen different states on its four output lines. The last three lines: B, C, and D, drive decoder U10 which produces an output on one of eight output lines for each of the eight different states of the inputs: B, C, and D.

Seven of the eight single line outputs of decoder U10 are used to select display digits directly. The address to the DCU's of A103 however, is a one-of-four line code, plus an odd-even code on a fifth line. The one-of-four line code is obtained by combining successive outputs of decoder U10 in groups of two in the four AND gates of U11. The odd-even code is simply the A input to U10.

### Display Decoder, Driver, and Leading Zero Suppression Circuits (U2, U4, U8)

The BCD to 7-segment decoder is included in U8. It directly supplies the cathode currents to the segments of the display digits which must be illuminated to display the number given by the BCD code. Additional inputs to U8 allow all outputs to be activated simultaneously (Lamp Test which displays all 8's), all outputs turned off simultaneously (BI/RBO which blanks the display), or the output blanked if the BCD input is zero (RBI). This last input is used in leading zero suppression.

The anode currents of the seven display digits are supplied by the seven individual digit drivers Q1-Q7. These drivers are turned on in sequence by outputs 1 through 7 of U10, and effectively apply the +5 volt adjustable supply to the anodes of the display digits. The segment currents are then determined by the segment drive outputs of U8, and the seven resistors in the output lines. (Active outputs are driven to ground so output currents will be determined by the value of the series resistors.) Corresponding segments of all display digits are wired in parallel, with all seven display digits being driven simultaneously by the 7-line decoder. Only one of these digits is supplied anode current by the digit drivers at any given time. The correct BCD input to U8 is selected by address decoders on the Count Chain (A103).

The zero suppression circuits cause all digits to the left of the first non-zero display to be blanked. Outputs of decoder U10 are processed in U2, U4, U8, and U12, to produce this result.

Decoder outputs of U10 occur in regular time sequence 0 through 7. Defining the interval in which output 0 is active as TF0 (Time Frame 0), then intervals TF0, TF1 ..... TF7, are of equal length, and occur in a regular repetitive sequence. Display digits are driven in Time Frames TF1 - TF7. The zero suppression latches are reset in TF0 of each sequence. The BCD output from A103 is coded to be always zero in TF0. This is decoded in data detector U2 to produce a high at the set input to the U4B latch. U9A output, and U10 TF0 output, are combined in U3 and U7 to produce a reset input to U4B at TF½ (the second half of TF0). U4B is then always reset at the beginning of the TF1-TF7 sequence. During this sequence, the DCU outputs of A103 are addressed and read out in sequence: 10 GHz, 1 GHz ... 100 kHz. If any of these BCD outputs are non-zero, detector U2 immediately sets U4B. U4B is then reset until the left-most non-zero digit of the display appears after which it remains set through the remainder of each display sequence. This flip-flop is used to remove the suppression when all digits are zero, otherwise the display would disappear completely if there were no input to the counter (zero frequency). The narrow MUX clock is applied to the non-zero data detector via U12 to disable the detector during clock pulses, so switching transients do not cause problems.

Flip-flop U4A controls the zero suppression directly. If U4B is in the set state at the end of a display sequence, then U4A is reset by the clock pulse at TF½ of the next sequence. If U4B is in the reset state at the end of TF7, then U4A is set at TF½ of the next sequence. If non-zero data occurs in a display sequence, U4A is set and enables zero suppression in the next sequence. If all data is zero through a sequence, U4A is set and disables zero suppression in the next sequence. Assuming that many display sequences occur for each set of BCD data, then all zero data receives no suppression, and all zeros are displayed, while non-zero data has leading zeros suppressed.

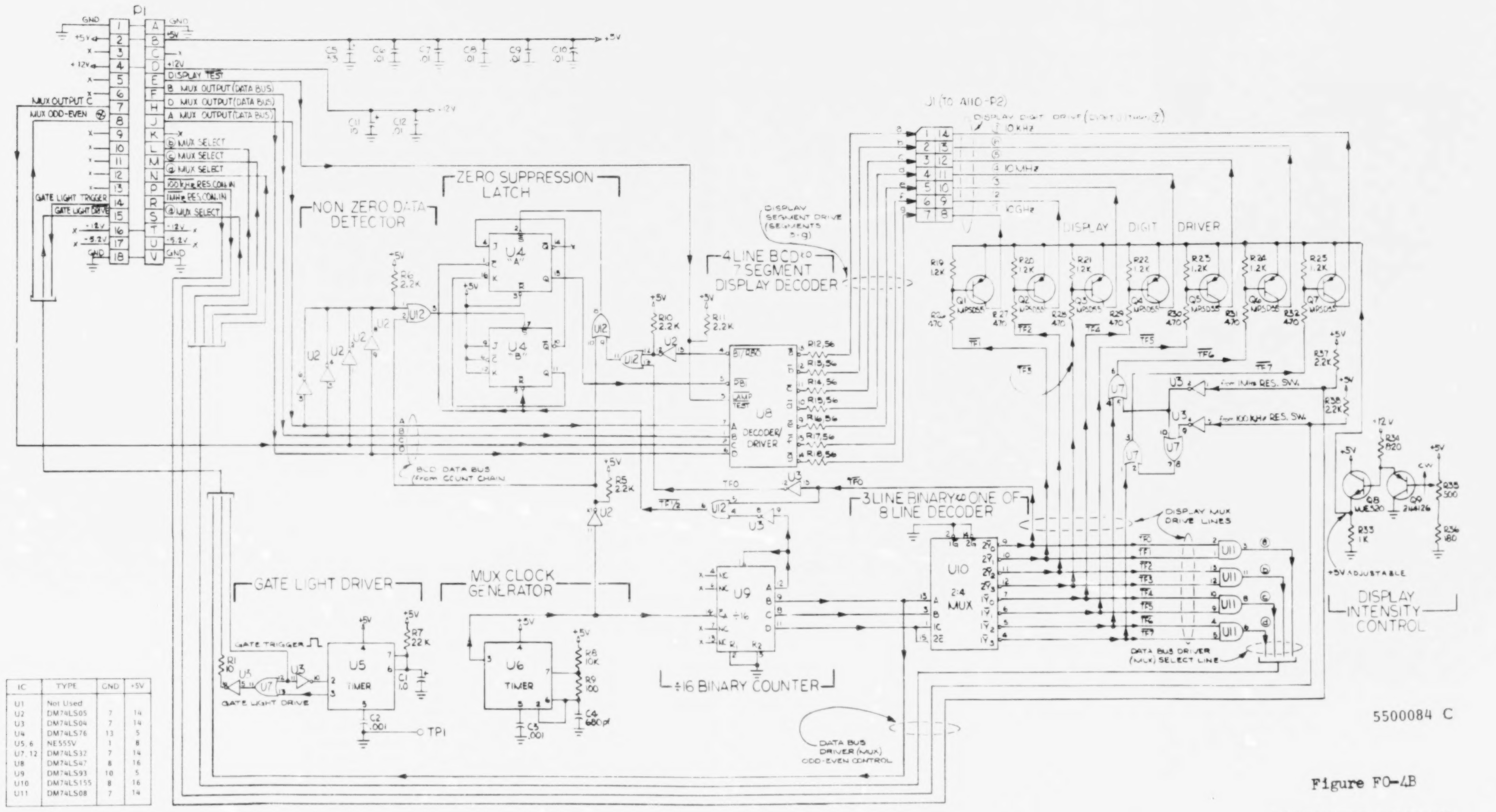
U4A enables zero suppression in its reset state by applying the low Q output to the ripple blanking RBI input of U8. With this input low, all decoder outputs are shut off when the data is low and the BI/RBO output is also low. When ever data becomes non-zero, BI/RBO goes high and sets U4A, removing the RBI input enable. This can only be again enabled at the start of a following sequence when U4A may be reset.

### Gate Indicator Driver (U3, U5, U7)

The front panel **GATE** indicator is driven directly by OR gate U7C in response to the gate trigger from A105. A second input to this gate is obtained from U5 which is also set by the gate trigger via inverter U3E. U5 is a one-shot whose period is set to about 30 ms. The drive pulse to the indicator in response to each gate trigger is then of sufficient duration to be visible, even for very short gate times.

Figure FO-4A

Component Locator
and
Descriptive Information
COUNT CHAIN CONTROL (A102)


P1
GND
+5V
+12V
MUX OUTPUT C
MUX ODD-EVEN
GATE LIGHT TRIGGER
GATE LIGHT DRIVE
-12V
-5.2V
DISPLAY TEST
B MUX OUTPUT (DATA BUS)
D MUX OUTPUT (DATA BUS)
A MUX OUTPUT (DATA BUS)
Ⓑ MUX SELECT
Ⓒ MUX SELECT
Ⓓ MUX SELECT
100 kHz RES. CON. IN
1 MHz RES. CON. IN
Ⓐ MUX SELECT
NON ZERO DATA DETECTOR
ZERO SUPPRESSION LATCH
U4 "A"
U4 "B"
4 LINE BCD TO 7 SEGMENT DISPLAY DECODER
U8 DECODER/ DRIVER
DISPLAY SEGMENT DRIVE (SEGMENTS a-g)
J1 (TO A110-P2)
DISPLAY DIGIT DRIVE
10 KHz
10 MHz
1 GHz
DISPLAY DIGIT DRIVER
from 1 MHz RES. SW.
from 100 KHz RES. SW.
BLC DATA BUS (FROM COUNT CHAIN)
3 LINE BINARY TO ONE OF 8 LINE DECODER
U10 2:4 MUX
DISPLAY MUX DRIVE LINES
DATA BUS DRIVER (MUX) SELECT LINE
DISPLAY INTENSITY CONTROL
+5V ADJUSTABLE
GATE LIGHT DRIVER
GATE TRIGGER
GATE LIGHT DRIVE
U5 TIMER
MUX CLOCK GENERATOR
U6 TIMER
TP1
÷16 BINARY COUNTER
DATA BUS DRIVER (MUX) ODD-EVEN CONTROL

| IC | TYPE | GND | +5V |
|---|---|---|---|
| U1 | Not Used | | |
| U2 | DM74LS05 | 7 | 14 |
| U3 | DM74LS04 | 7 | 14 |
| U4 | DM74LS76 | 13 | 5 |
| U5, 6 | NE555V | 1 | 8 |
| U7, 12 | DM74LS32 | 7 | 14 |
| U8 | DM74LS47 | 8 | 16 |
| U9 | DM74LS93 | 10 | 5 |
| U10 | DM74LS155 | 8 | 16 |
| U11 | DM74LS08 | 7 | 14 |

5500084 C

Figure FO-4B

SCHEMATIC DIAGRAM
COUNT CHAIN CONTROL (A102)

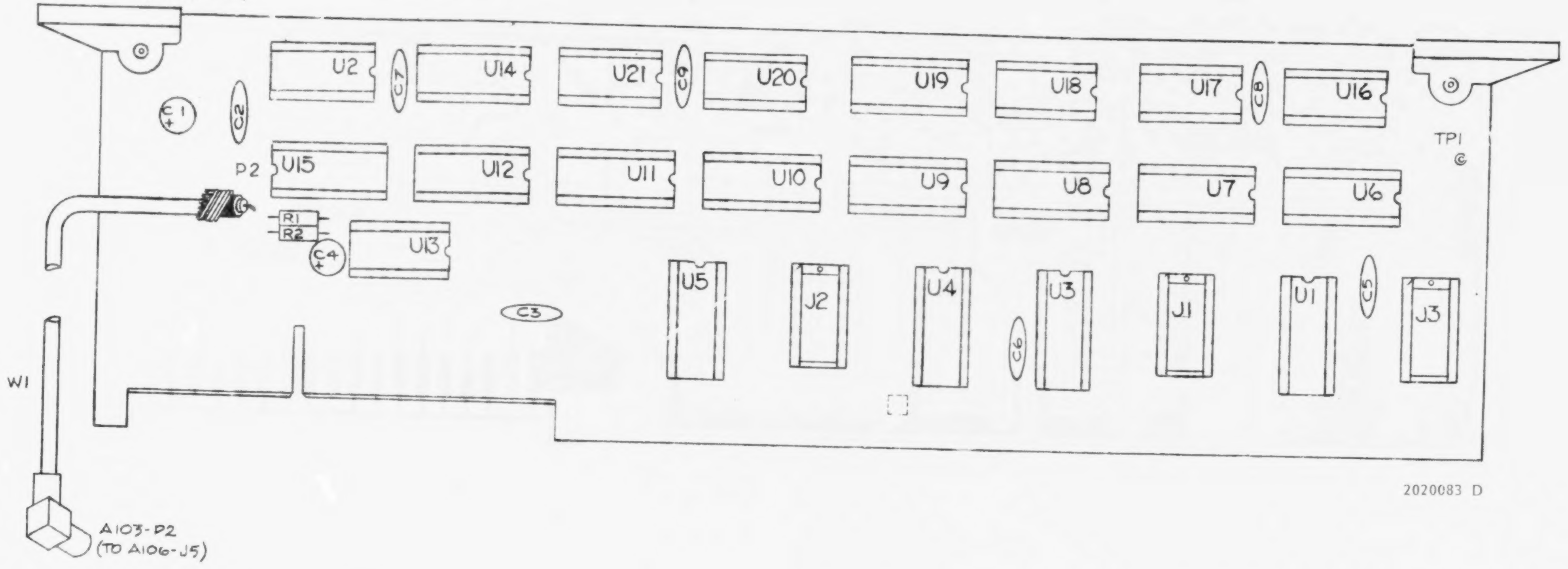


Figure FO-5A
Component Locator
and
Descriptive Information
COUNT CHAIN (A103)

## COUNT CHAIN (A103)

### General

Count Chain board A103 accumulates the counts provided by the output of High Frequency board A106, and on command, stores this BCD information in a separate storage unit. A multiplexer scans the information one digit at a time, and presents the BCD digits serially on a four line output bus. (For Option P4, the same information is presented in parallel form to the rear panel BCD Output connector.) The last three DCU's of the counting chain may be preset before normal counting begins.

The 451 Counter measures frequencies by dividing the input frequency in cascaded Decimal Counting Units (DCU's) for a precisely determined gate time. The number of accumulated counts, divided by the gate time, gives the frequency directly. The first DCU is on A106, and is followed by seven additional DCU's on this board. Each DCU has a four-line BCD output to show its accumulated count. These BCD outputs are decoded and drive the front panel display which shows the value of the digits accumulated by each of these DCU's.

### Counting Chain (U16-21)

The counting chain incorporates seven DCU's. The first two are higher speed than the remaining five, as they must operate at higher frequencies. Except for the first DCU, the D output of each DCU directly drives the clock input of the next DCU. The first DCU is presettable by the 1 ms gate command. When this command is not activated, the DCU is held in the "9" state. The DCU carry from the High Frequency board (A106) then bypasses the first DCU and directly clocks the second DCU. When the 1 ms gate command is activated, the preset is removed, and the DCU carry clocks the first DCU which clocks the second. In this state, the first DCU is effectively placed in the count chain. The last three DCU's may be preset to any desired number by applying a load command before normal counting begins. This is used to add the Converter local oscillator frequency to the counting chain to obtain the actual input frequency in Band B.

### Storage Unit (U6-12, U14)

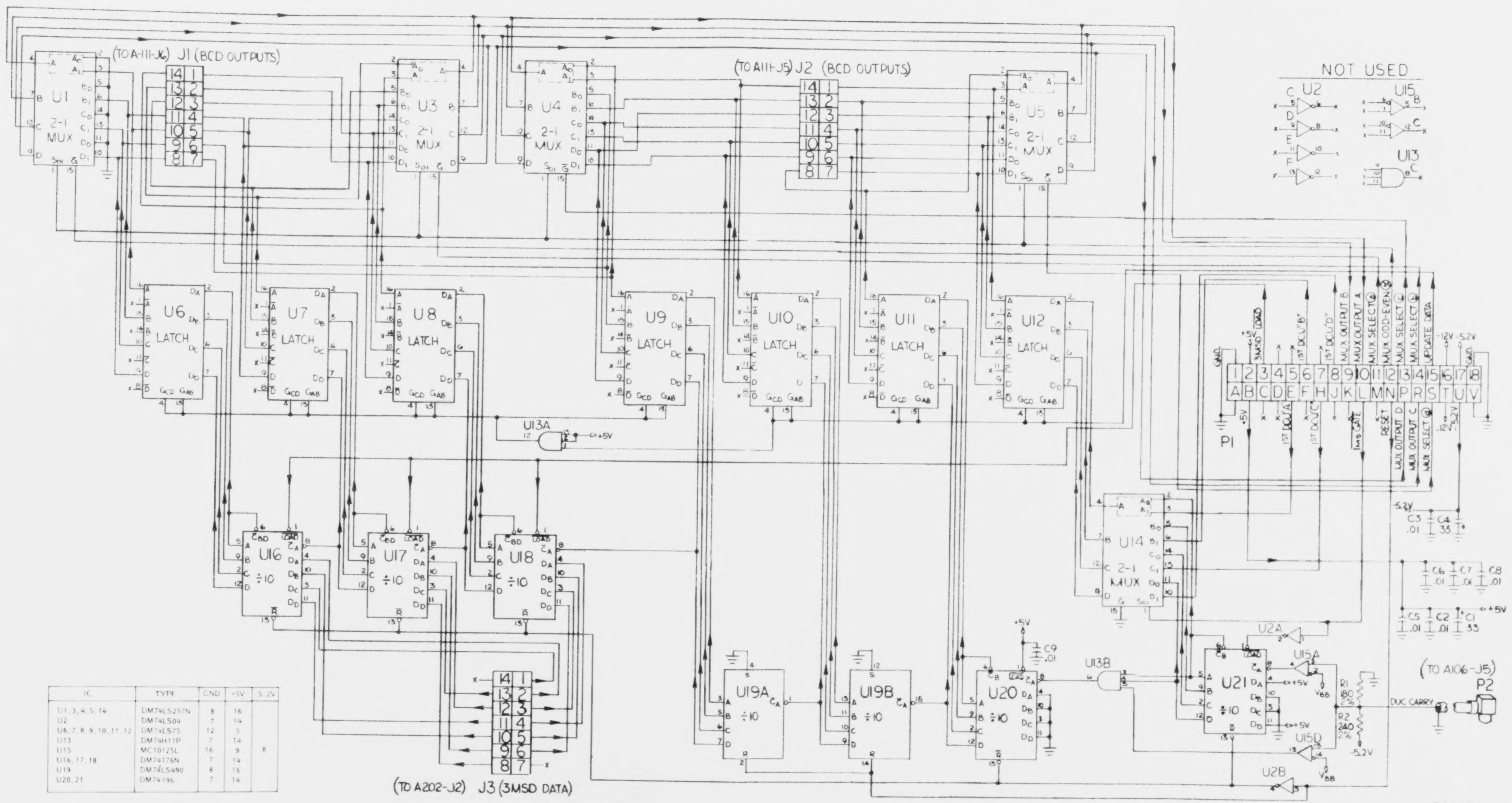
Seven 4-bit latches are provided which store the information from the DCU's. The last six are driven directly from the BCD information of each corresponding DCU. The first one is driven from a data selector multiplexer which is controlled by the 1 ms gate command. When this command is not activated, the data selector presents the BCD information from A106 to the latch. When the 1 ms gate command is activated, the data selector selects the BCD information from the first DCU on this board.

Storage Unit (U6-12, U14)

Seven 4-bit latches are provided which store the information from the DCU's. The last six are driven directly from the BCD information of each corresponding DCU. The first one is driven from a data selector multiplexer which is controlled by the 1 ms gate command. When this command is not activated, the data selector presents the BCD information from A106 to the latch. When the 1 ms gate command is activated, the data selector selects the BCD information from the first DCU on this board.
A load command to all latches, causes the DCU information to be stored and held until the next load command. All information from the counting chain to the balance of the counter, is obtained from these latches.

### Data Output Multiplexer (U1, U3-5)

The multiplexer converts the parallel BCD information located in the latches, to the serial form necessary to drive the front panel display. Each multiplexer has tri-state outputs — this means that the multiplexer can be gated into an active or passive state. In the passive state, the output is a high impedance which does not respond to the input, thereby allowing the output to be controlled by another IC. Each IC contains four separate channels, with one output and two inputs per channel. A select input to each IC allows one or the other of the inputs to be transferred to the output. The parallel BCD information from the latches is directly applied to the multiplexer inputs. An input select line (MUX Odd/Even), combined with a four-line gating bus (MUX Select Bus), serially selects this BCD information and places it on the multiplexer outputs which are tied together. The end result is serial BCD information which corresponds to the input frequency.



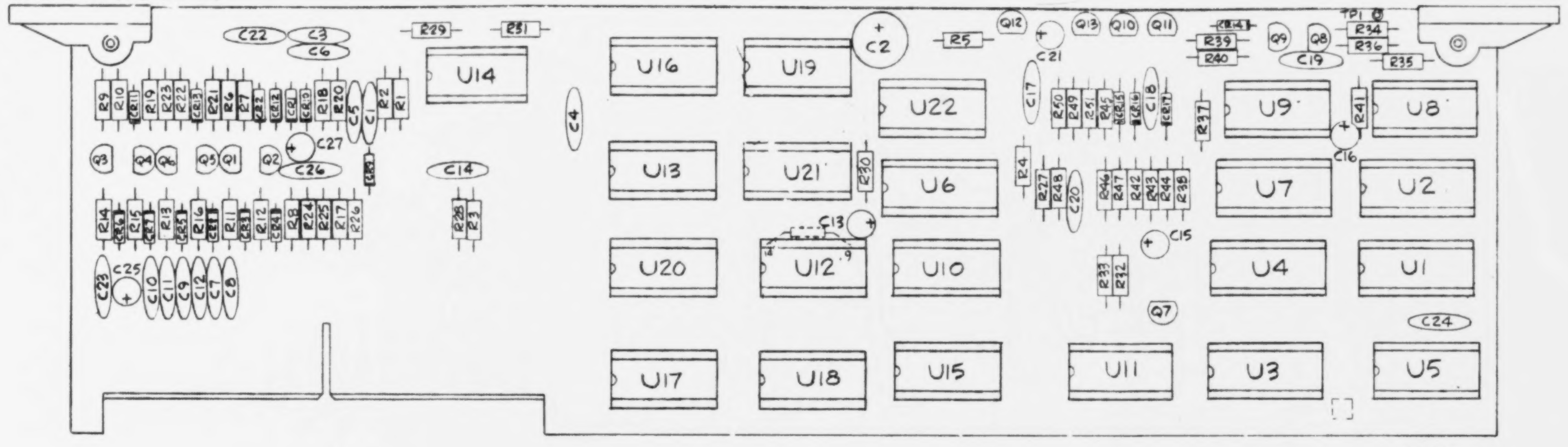
(TO A111-J6) J1 (BCD OUTPUTS)
(TO A111-J5) J2 (BCD OUTPUTS)
(TO A202-J2) J3 (3 MSD DATA)
U1 2-1 MUX
U3 2-1 MUX
U4 2-1 MUX
U5 2-1 MUX
U14 2-1 MUX
U6 LATCH
U7 LATCH
U8 LATCH
U9 LATCH
U10 LATCH
U11 LATCH
U12 LATCH
U13A
U13B
U16 ÷10
U17 ÷10
U18 ÷10
U19A ÷10
U19B ÷10
U20 ÷10
U21 ÷10
U2A
U2B
U15A
U15D
NOT USED
U2
U15
U13
P1
P2
(TO A106-J5)
DUC CARRY
R1 80
R2 240
C1 33
C2 .01
C3 .01
C4 33
C5 .01
C6 .01
C7 .01
C8 .01
C9 .01
+5V
-5.2V

| IC | TYPE | GND | +5V | -5.2V |
|---|---|---|---|---|
| U1, 3, 4, 5, 14 | DM74LS257N | 8 | 16 | |
| U2 | DM74LS04 | 7 | 14 | |
| U6, 7, 8, 9, 10, 11, 12 | DM74LS75 | 12 | 5 | |
| U13 | DM74H11P | 7 | 14 | |
| U15 | MC10125L | 16 | 9 | 8 |
| U16, 17, 18 | DM74176N | 7 | 14 | |
| U19 | DM74LS490 | 8 | 16 | |
| U20, 21 | DM74196 | 7 | 14 | |

5500083 A

Figure FO-5B

SCHEMATIC DIAGRAM
COUNT CHAIN (A103)



2020074 J

## CONTROL (A104)

### General

The primary function of this unit is to control and step the counter through the sequence of operations required to measure the frequency of the input signal to the counter.

As with the central processing unit of a computer, generation of this sequence of commands to various portions of the counter is timed by an internal clock. The sequence may be modified by external control inputs, hence the outputs of most panel controls on the counter feed directly to this unit (TEST, BAND, RESET, etc.). Reset always returns the sequence immediately to a fixed starting point.

### Control Sequence Generator (U1-5)

This unit produces control signals in sequence on one of sixteen output lines. U5 is a straight scale-of-sixteen binary counter which advances one state each time a clock pulse is applied to its input. The four outputs A, B, C, and D, are applied to two 3-8 line decoders (U3,U4) to produce an output on one of 16 lines corresponding to each of the sixteen possible states of binary counter U5. A reset signal to U5 returns the unit to the start of the sequence with the "0" output line active. A disable input to the decoders allows all outputs to be deactivated at any point in the sequence. This is used during the clock pulse or the reset input to U5 to prevent false outputs on any decoder lines from occurring during times when the counter outputs are in transistion between states.

Flip-flop U2A is used to indicate whether the sequence is in one of the states "0" through "9" or in one of the states "10" through "15". After state "9", the frequency measurement is already complete but not yet displayed. The reaction to external interrupts is then different in these two cases.

Flip-flops U1A and U1B are used to produce a much longer than normal step in the control sequence. This allows extra time to read data from the DCU's of the Count Chain in A103 through a multiplexer into latches which hold this data. Output state "11"" sets flip-flop U1A which immediately gates off all the decoder outputs via gates U10B, U9B, U11A, and U11B. The sequence generator then operates at full speed in states "12" through a second "12". Flip-flop U1B is set by the D output of U5 while going into state "8", which reactivates the decoder outputs. The output during state "12" is able this time to reset both U1A and U1B, and return the sequence generator to normal operation. The DATA UPDATE output during this long step of the sequence is obtained from U1A rather than from the decoder outputs.

Decoder outputs "13" and "14" are combined in U16 to produce a Print Command pulse twice the duration of the normal sequence outputs.

The control sequence may be frozen in any state by interrupting the clock input to binary counter U5.

### Control Sequence

There are 16 output lines from the decoders which are energized in sequence each time the counter repeats a measurement cycle. The operations which correspond to commands on each of these lines 0-15 are listed in Table 4-6.

Any of the normal times listed the Table may be extended by interrupting the sequence clock. The times listed as variable in the Table are controlled by internally generated interrupt signals. With Programming Option P4, such an interrupt may be applied from outside the counter. This might occur with a printer, which must freeze the data in the counter until printing is complete. Other interrupts may be generated internally, depending upon the state of the input signal to the counter.

### Control Sequence Reset or Interrupt Conditions

The Sequence Generator is reset to its "0" state in a variety of conditions where a measurement has started but cannot be successfully completed. The reset then prevents erroneous data from being displayed or sent out to other remote equipment. The actions that cause these resets include: externally controlled changes of the mode in which the counter operates (band change, Test, etc.), or large changes in the input signal itself before a successful measurement can be completed. The sequence can also be interrupted or reset by direct external commands.

Events which cause both reset of the sequence to "0" and Converter recycle (plus immediate zero display), are as follows:

a. Counter power turn-on.
b. Switch to Band B.
c. End Test in Band B.
d. Reset commands externally or manually applied.

Other events which cause the sequence to be reset to "0":

a. Change of RESOLUTION controls.
b. Switch to Band A.
c. Start Test.
d. End Test in Band A.
e. Start-cycle command from external source.
f. Converter lock or unlock in Band B during sequence "0" - "9".
g. PRF limit signal changes state (input signal appears or drops out) during sequence "0" - "9".

A number of conditions also cause the sequence to be inhibited:

a. A direct Sequence Inhibit command from an external source.
b. Operation of the Display Time Generator. This produces a variable time inhibit controlled by the SAMPLE RATE control or a permanent inhibit with the control at HOLD. A reset (external or manual) command over-rides this signal and causes a single sequence before the inhibit is re-established.
c. Operation of the Gate Generator (A105). During Sequence "8" if the counter is in Test or locked to an input signal, the Gate Generator inhibits the sequence until the prescribed gate time is accumulated. Input signal dropout removes this inhibit unless the unit is in the Test mode.
d. PFR limit signal appears (input signal level above threshold) in Band B, but Converter LOCK absent. A delay is produced before sequence continues (or resets) to see of Lock will soon be achieved.
e. LOCK lost in Band B. Time is allowed for relock to a measurable input signal before a reading of zero is produced. This prevents zero readings when lock is broken, even though a measurable input is present continuously.

### Reset Pulse Trigger Generators

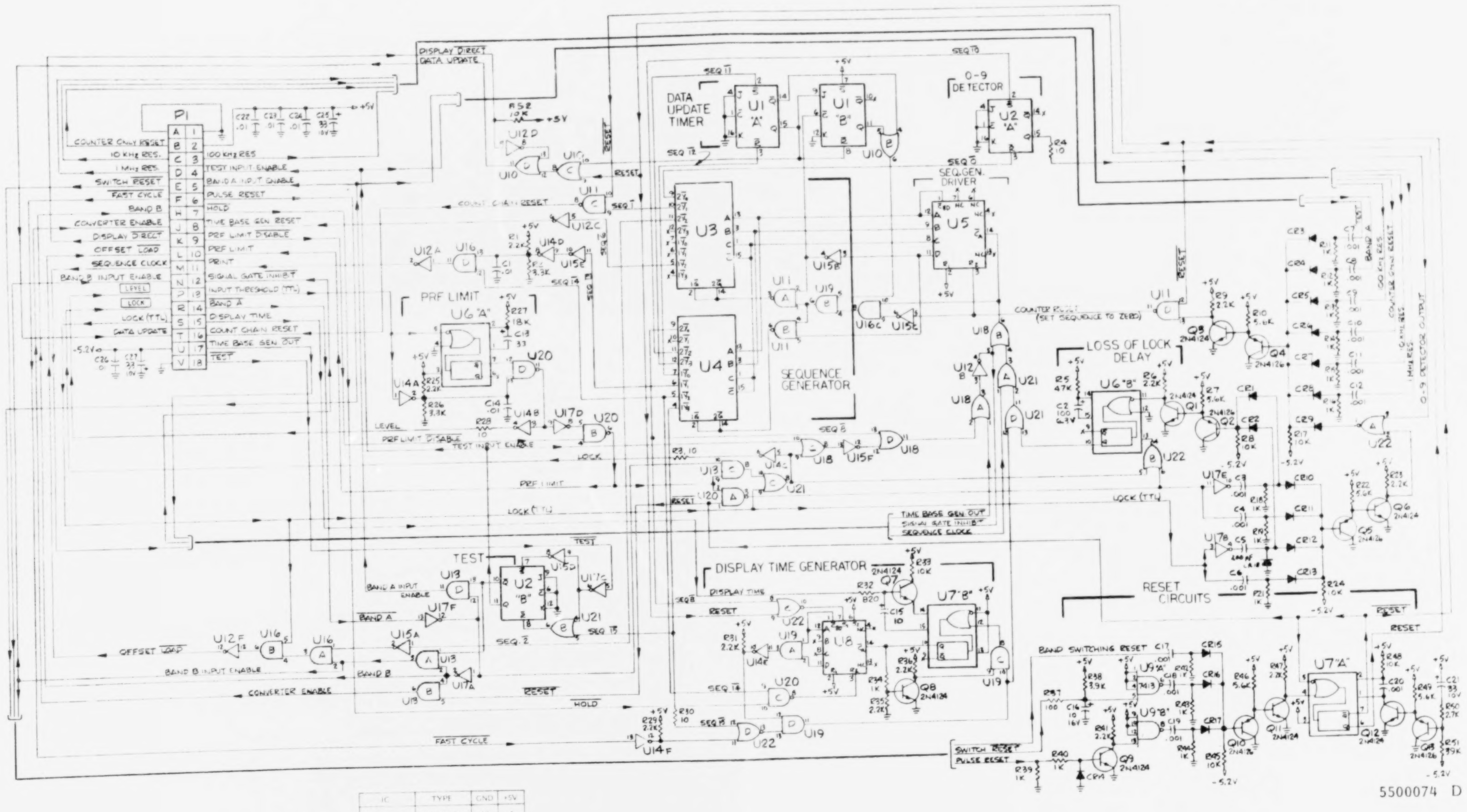
A large proportion of A104 consists of circuits which reset the sequence generator or other portions of the counter. The triggers which operate the reset generators are formed from the various inputs in the same way. The input signals are step functions which are differentiated in RC networks (C16, R37, for example), and coupled through diode to a common two transistor output stage (Q10, Q11, for example). The TTL compatible output trigger then drives the IC reset generator or gate.

Six inputs to C7-C12 are combined in diodes CR3 - CR8 and output stage Q3, Q4 to reset the sequence generator through gate U11D. Four additional inputs to C3-C6 are combined in CR10-CR13 and output stage Q5, Q6 to drive OR gate U22A. During sequence states "0" - "9", this gate drives the first network through CR9 and resets the sequence generator if any input to C3-C6 occurs during states "0"-"9".

Three inputs to C17 - C19 drive a similar network through CR15 - CR17, and Q9, Q9. These trigger the reset generator one-shot U7A, which produces a uniform pulse about 5 µs in duration. This pulse resets the sequence generator, the display generator, the lock delay generator, and externally the Count Chain and Converter. The Count Chain immediately generates and displays a zero.

The inputs to C18 and C19 are obtained from Schmitt triggers in U9. Inputs to U9 are slow rise signals which are changed to single fast steps by the threshold circuits of U9.

Figure FO-6A
Component Locator
and
Descriptive Information
CONTROL (A104)

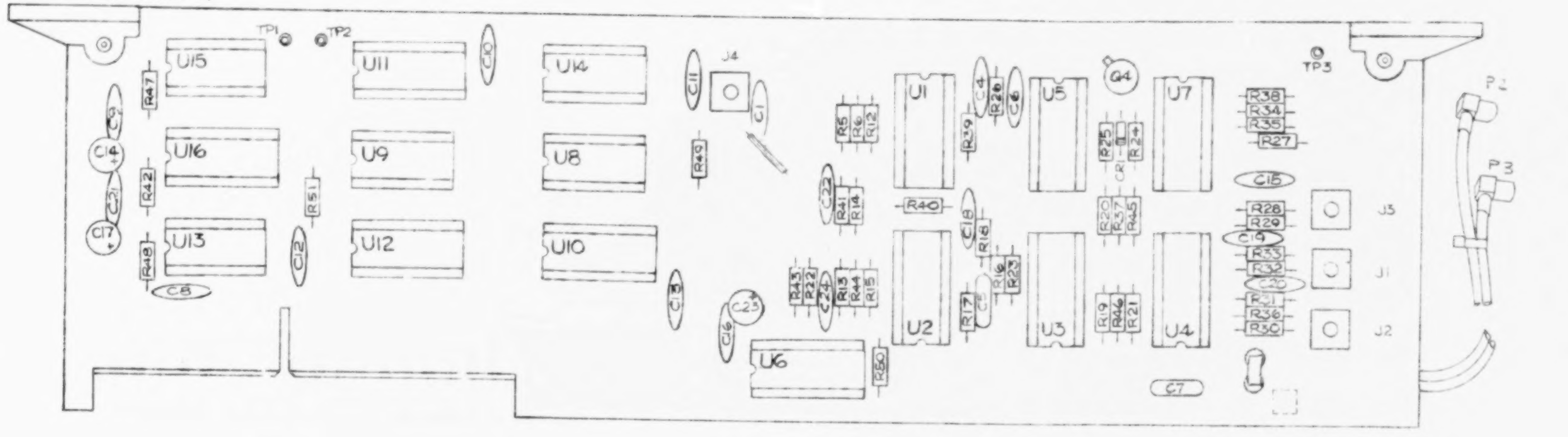

P1
COUNTER ONLY RESET
10 KHz RES.
1 MHz RES.
SWITCH RESET
FAST CYCLE
BAND B
CONVERTER ENABLE
DISPLAY DIRECT
OFFSET LOAD
SEQUENCE CLOCK
BAND B INPUT ENABLE
LEVEL
LOCK
LOCK (TTL)
DATA UPDATE
100 KHz RES
TEST INPUT ENABLE
BAND A INPUT ENABLE
PULSE RESET
HOLD
TIME BASE GEN RESET
PRF LIMIT DISABLE
PRF LIMIT
PRINT
SIGNAL GATE INHIBIT
INPUT THRESHOLD (TTL)
BAND A
DISPLAY TIME
COUNT CHAIN RESET
TIME BASE GEN OUT
TEST
DISPLAY DIRECT DATA UPDATE
DATA UPDATE TIMER
0-9 DETECTOR
SEQ GEN DRIVER
SEQUENCE GENERATOR
PRF LIMIT
LOSS OF LOCK DELAY
TEST
DISPLAY TIME GENERATOR
RESET CIRCUITS
BAND SWITCHING RESET CKT

5500074 D

BOX ▭ DENOTES FRONT PANEL INDICATOR.
ALL DIODES ARE 1N4154.

| IC | TYPE | GND | +5V |
|---|---|---|---|
| U1, 2 | DM74LS76 | 13 | 5 |
| U3, 4 | DM74LS155 | 8 | 16 |
| U5 | DM74LS93 | 10 | 5 |
| U6, 7 | DM9602N | 8 | 16 |
| U8 | DM74LS90 | 10 | 5 |
| U9 | DM74LS13 | 7 | 14 |
| U10, 18, 21 | DM74LS32 | 7 | 14 |
| U11, 20 | DM74LS00 | 7 | 14 |
| U12, 15, 17 | DM74LS04 | 7 | 14 |
| U13, 16, 19 | DM74LS08 | 7 | 14 |
| U14 | DM74LS05 | 7 | 14 |
| U22 | DM74LS02 | 7 | 14 |

Figure FO-6B
SCHEMATIC DIAGRAM
CONTROL (A104)



## GATE GENERATOR (A105)

General

The primary function of this unit is to produce the gate signal which controls the time intervals over which the input to the counter is accumulated. It also produces the 100 kHz Control Sequence Clock, and a 200 MHz Test signal. These outputs are all based on 200 MHz and 10 MHz references supplied from other portions of the counter.

Gate and Enable Flip-Flops (U2A/B).

The flip-flops are dual ECL types, both clocked by the same 200 MHz reference signal. The Gate Flip-flop controls the main counter signal gate directly, while the Enable Flip-flop determines which cycle of the 200 MHz clock will trigger the Gate Flip-flop.

The enable signal to the Enable Flip-flop, is derived from the counter input threshold circuit, and is present only at times when an input signal of adequate amplitude is present. This signal is combined with a signal from Control board A104, which indicates that the counter is in the correct part of its cycle to actually measure the input signal frequency. The rise time of the enable signal is faster than the clock period, so the Enable Flip-flop will always settle definitely into one of its two stable states when any individual clock pulse arrives.

The output of the Enable Flip-flop is applied to the enable input of the Gate Flip-flop which is triggered to the corresponding state by the next 200 MHz clock pulse. Transistions of the Gate Flip-flop occur only at a defined trigger point on the clock pulse, which is timed very accurately ($<<$ 1 ns from periodic 200 MHz). The output of the Enable Flip-flop is also combined with the output of the Time Base Flip-flop (U2B). This allows only a specified number of clock pulses to occur during the gate time of each measurement cycle of the counter. Accumulated gate times are: 1 ms or 100 μs (4 ms or 400 μs in Band A). The Gate control signal is applied via a 50 ohm cable to the signal gate on A106.

Time Base Flip-Flop (U3B).

This is another fast ECL flip-flop. It is clocked by a 200 MHz signal, slightly delayed from that driving the Enable and Gate Flip-flops. The delay allows the Gate Flip-flop (triggered by the normal clock), to control the delayed clock during the same clock period in which the Gate Flip-flop changes state. The clock delay and propagation delay through the flip-flop, are approximately equal. The Time Base Flip-flop is reset at the beginning of each measurement cycle, removing the disable signal applied by it, to the Gate Flip-flop.

During the gate enable portion of the counter control sequence, the Gate Flip-flop is controlled by the input threshold circuits via the Enable Flip-flop and the 200 MHz clock. Each time the Gate Flip-flop opens the Signal Gate, the 200 MHz delayed clock is also applied to the Time Base Accumulator and to the Time Base Flip-flop clock input. The clock pulse which opens the signal gate is ignored. All pulses which occur during a Signal Gate open period are recognized, including the one which closes the Gate. Coincidence circuits in the Time Base Accumulator produce signals when N-4 and N-3 clock pulses have been applied to the Accumulator. N is the number of clock periods required to produce the desired accumulated gate time. The N-4 signal is applied to the clock enable input, and the N-3 signal to the enable input of the Time Base Flip-flop. The N-2 clock pulse then actually triggers the Time Base Flip-flop to its set state. The delay already present in the delayed clock driving the accumulator, is extended by a delay network following the Time Base Flip-flop. The disable signal from the Time Base Flip-flop to the Gate Flip-flop input is then delayed until after the N-1 normal clock pulse. The N clock pulse resets the Gate Flip-flop, and ends gate time for that measurement cycle.

Time Base Accumulator (U3A, U5, U10-12)

The Time Base Accumulator includes five DCU's (U5, U11, U12), preceded by a binary divider. The count capacity of this group is 200K clock pulses, each of 5 ns period, or 1 ms total. The last DCU may be removed from the string to permit a 100 μs gate time. In addition to the string of DCU's, a ÷4 unit is included between the first and second DCU's, which may be switched into or out of the chain. The ÷4 is included when operating in Band A, to increase the gate time by a factor of four. The input to A106 is divided by four before reaching the Signal Gate, so the gate time must be extended to cause the counter to read the input frequency directly.

A coincidence detector consisting of U7A, U8, U9, U14D, Q4, CR1, and the D output of U5, produces an output when all DCU's of the string are in state "9", and the ÷4 unit is in state "3". The first DCU of the string is preset to 9 originally, giving coincidence after N-2, rather than N-1 clock pulses to the first DCU. (Driving $C_{RD}$ input with the A, rather than the inverted A output, is equivalent to a preset 9.) Since the accumulator clock input is divided by two in binary U10A before the first DCU, coincidence output occurs on the N-4 input pulse.

Since coincidence occurs when all DCU's are at 9, and the ÷4 at 3, any one of them is effectively removed from the string if held at these counts. U12B has an external set 9 input to produce the shorter 100 μs gate time in this manner. This ÷4 unit may also be held at 3 by an external control signal (Band B or Test), but additional gating must be provided to pass the input signal around the stage, since the following DCU's still have to operate. This is accomplished in U8B, which transmits either the input or output of U10 to the input of U11A.

The ÷2, and the first DCU of the Accumulator, are fast ECL circuits, able to divide the 200 MHz clock to 10 MHz; the remaining circuits are TTL.

Band Select Circuits (U4B-D, U7B/C, U14A)

These circuits select one of the Band Threshold signals from either the Converter (Band B) or Prescaler (Band A), and processes this to control the Enable and Gate Flip-flops. U7C is simply a buffer/inverter which is driven by a level derived from the front panel BAND SELECT switch. The buffer output drives one input of U4B, while the inverter output drives one input of U4C, such that one of the pair U4B/U4C is always enabled, and one disabled. The inverting outputs of U4B and U4C are "ORed" together to drive one U4D input. The direct output of U4B is now a replica of the envelope of the signal to the selected input to the counter — being high if the signal is above threshold level, and low if the signal is less than threshold. The second input to U4D is high in the Test mode, so the Gate Flip-flop operates as if the 200 MHz Test signal is always above threshold level.

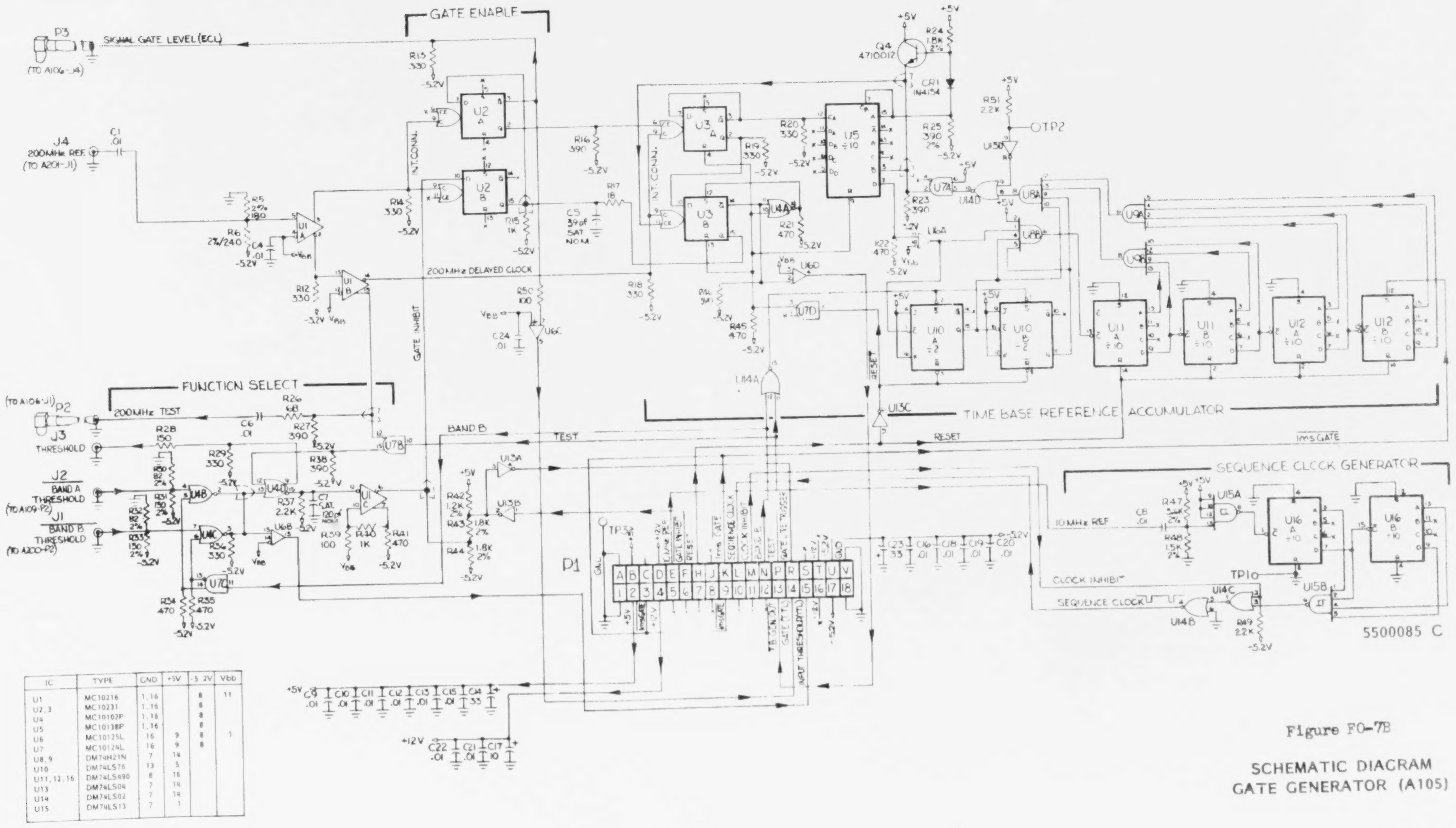
The output of U4D to the Enable Flip-flop goes low whenever the input signal to the counter is above threshold. A capacitor to ground slows the fall of this transistion without great effect on the risetime. The signal is squared up again in U1C to produce an Enable signal which is delayed from the rise of the input signal to threshold, but disappears without delay as the input drops below threshold. This delays counting of the input signal until irregularities on the rise of the RF pulse have died out.

Control Sequence Clock Generator (U14-16)

This circuit divides the input 10 MHz reference by 100 to form the 100 kHz Sequence Clock. The input accepts a wide variety of input levels and waveshapes, while producing a square wave of the proper level to drive U16. U15B gates the outputs of U16 to form 100 ns pulses at a 100 kHz rate. U14C allows the Clock to be gated by an external control level.

Figure FO-7A
Component Locator
and
Descriptive Information

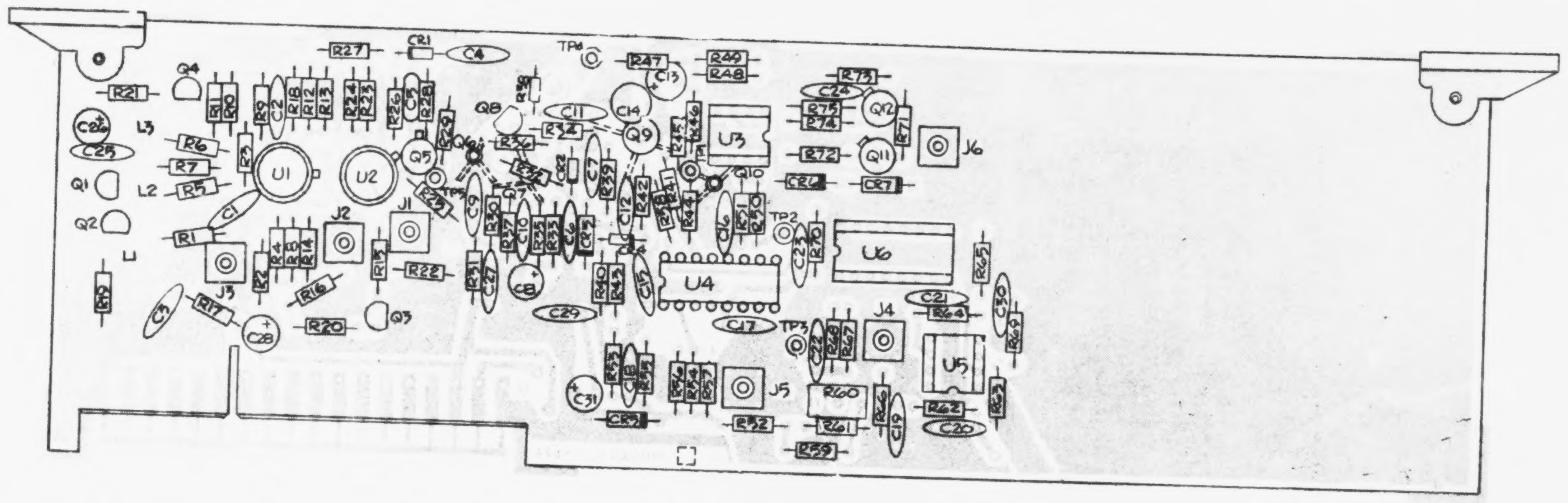
GATE GENERATOR (A105)


GATE ENABLE
P3
SIGNAL GATE LEVEL (ECL)
(TO A106-J4)
J4
200MHz REF.
(TO A201-J1)
C1 .01
R5 2% 180
R6 2%/240
C4 .01
-5.2V
VBB
U1 A
U1 B
U1 C
R12 330
R13 330
R14 330
U2 A
U2 B
INT. CONN.
R15 1K
R16 390
R17 18
C5 39pf SAT NOM.
200MHz DELAYED CLOCK
R18 330
U3 A
U3 B
R19 330
R20 330
R21 470
U4A
U5 ÷10
Q4 4710012
+5V
R24 1.8K 2%
CR1 1N4154
R25 390 2%
R51 2.2K
TP2
U13D
R23 390
R22 470
U7A
U14D
U8A
U8B
U9A
U9B
U6A
U6C
U6D
U7D
R50 100
C24 .01
R45 470
R46 390
GATE INHIBIT
U10 A ÷2
U10 B ÷2
U11 A ÷10
U11 B ÷10
U12 A ÷10
U12 B ÷10
U14A
RESET
U13C
TIME BASE REFERENCE ACCUMULATOR
1ms GATE
FUNCTION SELECT
(TO A106-J1) P2
200MHz TEST
C6 .01
R26 68
R27 390
U7B
J3
THRESHOLD
R28 150
R29 330
R38 390
J2
BAND A THRESHOLD
(TO A109-P2)
J1
BAND B THRESHOLD
(TO A200-P2)
R30 82 2%
R31 130 2%
R32 82 2%
R33 130 2%
U4B
U4C
U4D
U6B
R36 330
R37 2.2K
C7 SAT. 120pf NOM.
R39 100
R40 1K
R41 470
U7C
R34 470
R35 470
BAND B
TEST
+5V
R42 1.2K 2%
R43 1.8K 2%
R44 1.8K 2%
U13A
U13B
TP3
P1
GND
+12V
10MHz REF
GATE INHIBIT
RESET
1ms GATE
SEQUENCE CLOCK
CLOCK INHIBIT
BAND B
TEST
GATE, TE TRIGGER
TB GEN OUT
GATE (TTL)
INPUT THRESHOLD (TTL)
A B C D E F H J K L M N P R S T U V
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
C23 33
C16 .01
C18 .01
C19 .01
C20 .01
-5.2V
+5V
C9 .01
C10 .01
C11 .01
C12 .01
C13 .01
C15 .01
C14 33
+12V
C22 .01
C21 .01
C17 10
SEQUENCE CLOCK GENERATOR
10MHz REF
C8 .01
R47 5.6K 2%
R48 1.5K 2%
U15A
U16 A ÷10
U16 B ÷10
TP1
CLOCK INHIBIT
SEQUENCE CLOCK
U14B
U14C
U15B
R49 2.2K
5500085 C

| IC | TYPE | GND | +5V | -5.2V | Vbb |
|---|---|---|---|---|---|
| U1 | MC10216 | 1, 16 |  | 8 | 11 |
| U2, 3 | MC10231 | 1, 16 |  | 8 |  |
| U4 | MC10102P | 1, 16 |  | 8 |  |
| U5 | MC10138P | 1, 16 |  | 8 |  |
| U6 | MC10125L | 16 | 9 | 8 | 1 |
| U7 | MC10124L | 16 | 9 | 8 |  |
| U8, 9 | DM74H21N | 7 | 14 |  |  |
| U10 | DM74LS76 | 13 | 5 |  |  |
| U11, 12, 16 | DM74LS490 | 8 | 16 |  |  |
| U13 | DM74LS04 | 7 | 14 |  |  |
| U14 | DM74LS02 | 7 | 14 |  |  |
| U15 | DM74LS13 | 7 | 1 |  |  |

Figure FO-7B

SCHEMATIC DIAGRAM
GATE GENERATOR (A105)


R21
Q4
C26
L3
C25
Q1
Q2
L2
L1
R19
R6
R7
R5
R1
C1
C3
R17
C28
J3
R11
R10
R9
C2
R18
R12
R13
R24
R23
R26
C5
R28
R27
CR1
C4
R3
U1
U2
J2
J1
R4
R8
R14
R2
R16
R15
R22
R20
Q3
Q5
TP5
R29
Q6
Q7
Q8
R58
R32
R36
R34
R25
C9
R30
R37
C10
R35
R33
C6
CR3
CR2
C7
R39
C11
C14
Q9
C12
R42
R38
R41
R44
R45
R46
TP4
R47
C13
R49
R48
U3
Q10
C16
R51
R50
TP2
R31
C27
C8
R40
R43
C15
U4
C29
C17
TP3
R53
C18
R55
R56
R54
R57
C31
CR5
J5
R52
R60
R61
R59
C22
R68
R67
J4
R73
C24
R75
R74
Q12
R71
J6
R72
Q11
CR6
CR7
C23
R70
U6
R65
C21
R64
C30
R69
U5
R66
C19
R62
R63
C20

2020081 G

## HIGH FREQUENCY (A106)

The High Frequency board provides the initial signal processing and first decade of counting for the Direct Counter. It selects and processes one of three input signals: the Converter IF output, the Prescaler divide-by-four output, and the 200 MHz Test signal. BCD information and the divide-by-ten output from the first decade counting unit are sent from this board to the Count Chain board (A103) for further counting and display.

One of the three input signals is selected by enabling one of three differential amplifiers: U1B, U2A, or U2B. U1A provides additional gain for the Converter IF signal when input U1B is selected. Enabling of the appropriate amplifier is achieved by activating transistor Q2, Q3 or Q4, by TTL Band Select commands entering on P1.

The output of the input selector differentially drives the squaring circuit. Q5 is a current mirror, which is used as as an overdriven voltage-to-current converter. The collector current of Q5 drives the pulse forming network which begins with a wide-band, high-speed differential amplifier (Q6/Q7). The output of this differential amplifier drives Q8, which is used as a current switch. The resulting current square wave from Q8 drives inductor L4, producing a series of pulses — a positive pulse when Q8 turns on, and a negative pulse when Q8 turns off.

The pulse inverter is essentially a high-speed zero bias amplifier. Q9 performs this function by being biased at cut-off by diode CR4. In this mode, the amplifier not only inverts the positive pulses, but removes the unwanted negative pulses. The output of the pulse inverter drives the input of decade divider U4. The bias point for U4's input is established by a tracking bias supply (U3/Q10). The output of U3 is equal to the voltage on U4 pin 1, plus a fixed DC offset selected by resistor divider R47/R49. The divide-by-ten output of the decade divider is a 60/40 duty cycle ECL level signal called "DCU CARRY". The load resistor for this signal is located on the Count Chain board (A103) to provide a termination for the connecting co-ax cable.

The BCD output information is available on P1 pins 11-14. During a count cycle at high frequencies, this information is slew rate limited, therefore the actual output levels cannot be seen until the circuit comes to rest. After the circuit is finished counting, TTL level signals are present on these outputs. The decade divider is reset after the counting cycle is complete by a TTL reset signal on U4 pin 3. This signal comes into the board via P1 pin 10.

The gate signal (an inverted ECL level logic signal) enters the board at J4, and passes through U6. The first stage is an input buffer whose threshold signal (U6 pin 5) is derived from op amp temperature-compensated bias supply U5. U5's function is similar to U3 with the output tracking the reference voltage (U6 pin 11), plus some fixed offset supplied by voltage divider R59-R61. This accomodates slight changes in threshold which produce the effect of a change in gate width.

The gate output to the rear panel is supplied by the Gate Output Buffer, consisting of Q11, Q12, and associated circuitry.

Figure FO-8A
Component Locator
and
Descriptive Information
HIGH FREQUENCY (A106)

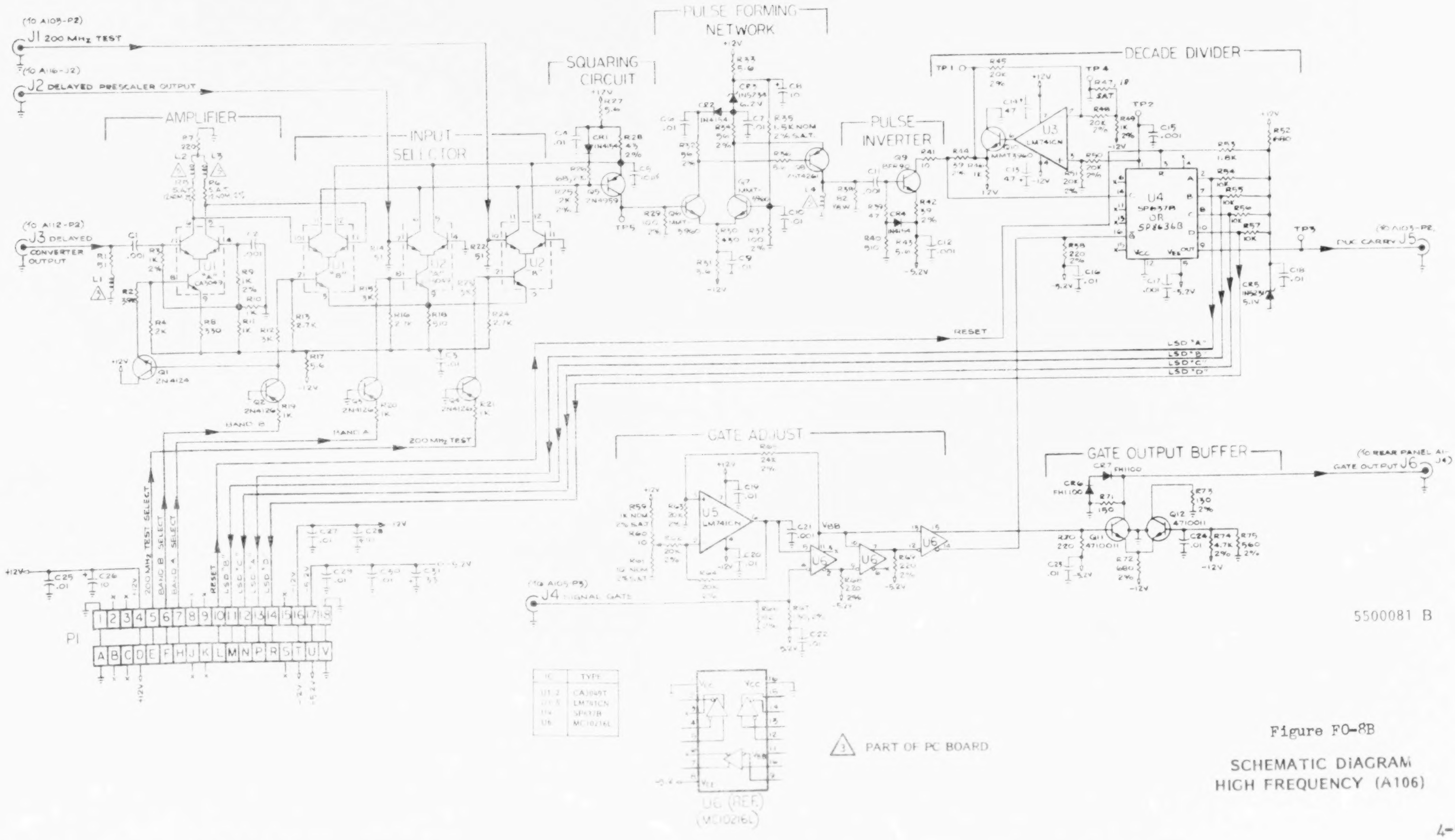
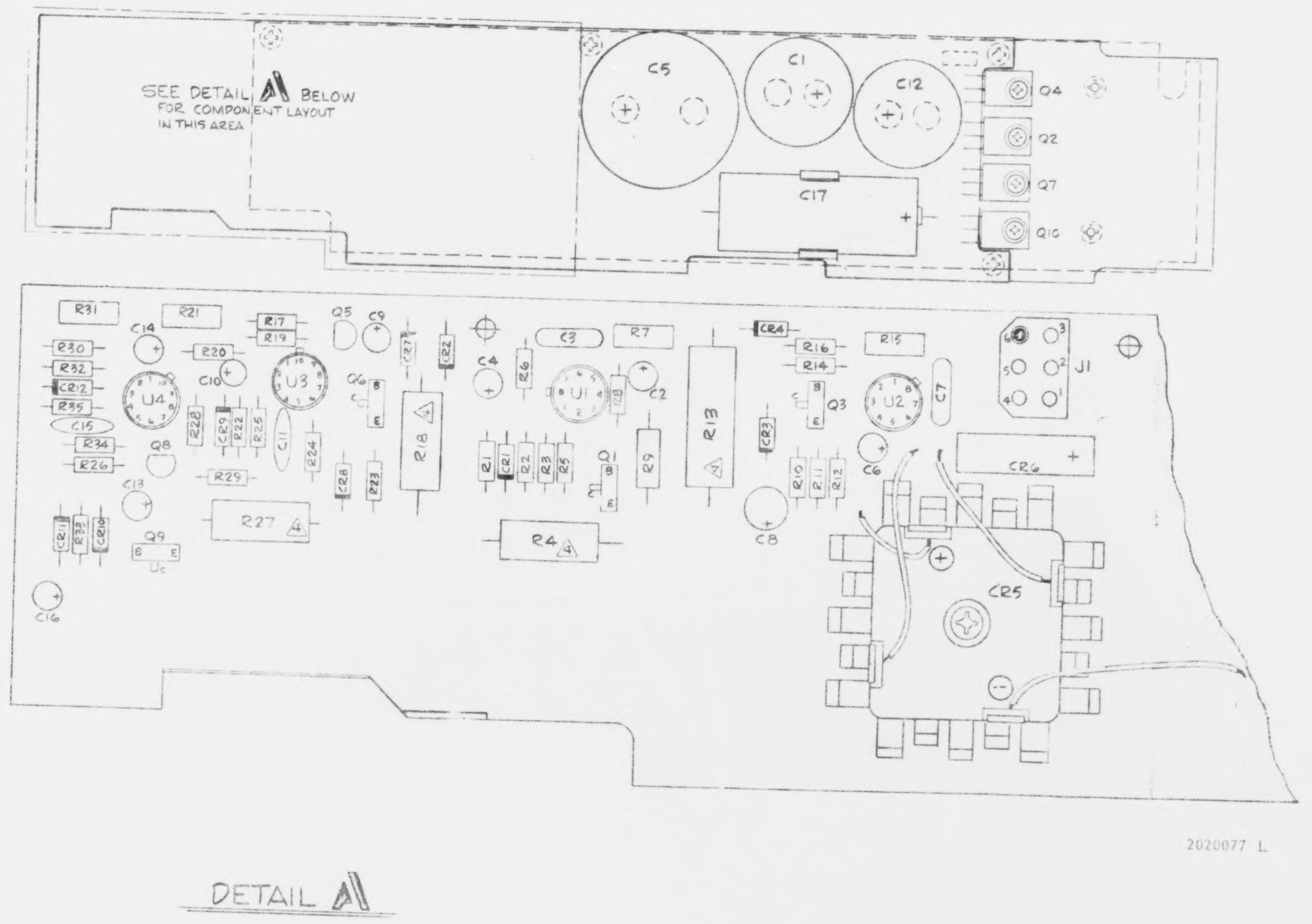

(TO A109-P2)
J1 200 MHz TEST
(TO A116-J2)
J2 DELAYED PRESCALER OUTPUT
(TO A112-P2)
J3 DELAYED CONVERTER OUTPUT
AMPLIFIER
INPUT SELECTOR
SQUARING CIRCUIT
PULSE FORMING NETWORK
PULSE INVERTER
DECADE DIVIDER
U4 SP637B OR SP2634B
LSD CARRY J5
RESET
LSD "A"
LSD "B"
LSD "C"
LSD "D"
BAND B
BAND A
200 MHz TEST
GATE ADJUST
U5 LM741CN
VBB
(TO A105-P3)
J4 SIGNAL GATE
GATE OUTPUT BUFFER
(TO REAR PANEL A1-J4)
GATE OUTPUT J6
P1
5500081 B
IC
TYPE
U1, 2
CA3049T
U3, 5
LM741CN
U4
SP637B
U6
MC10216L
PART OF PC BOARD
U6 (REF)
(MC10216L)

Figure FO-8B

SCHEMATIC DIAGRAM
HIGH FREQUENCY (A106)


SEE DETAIL A BELOW
FOR COMPONENT LAYOUT
IN THIS AREA
C5
C1
C12
C17
Q4
Q2
Q7
Q10
R31
R21
R17
R19
Q5
C9
C14
R30
R32
CR12
R35
C15
R34
R26
R20
C10
U4
U3
Q8
C13
R28
CR9
R22
R25
C11
R24
R29
R27
CR11
R33
CR10
Q9
C16
Q6
CR7
CR2
R18
CR8
R23
C4
R6
C3
R7
U1
R8
C2
R1
CR1
R2
R3
R5
Q1
R9
R4
R13
CR4
R16
R14
R15
Q3
CR3
U2
C7
C6
C8
R10
R11
R12
CR6
CR5
J1
2020077 L
DETAIL A

POWER SUPPLY (A1/A107)

The Power Supply furnishes all basic operating voltages required by the counter. The supply consists of two assembly groups:

(1) PC board A107 containing the rectifiers, filter capacitors, and regulator circuitry.

(2) Chassis mounted components (A1-) consisting of the power transformer (A1T1), primary wiring, POWER INPUT module (containing the fuse, voltage changing PCB, and power input connector), and the front panel POWER switch.

Circuit Description

The basic voltages required by the counter are: unregulated +18 Vdc, regulated +12 Vdc, -12 Vdc, +5 Vdc, and -5.2 Vdc.

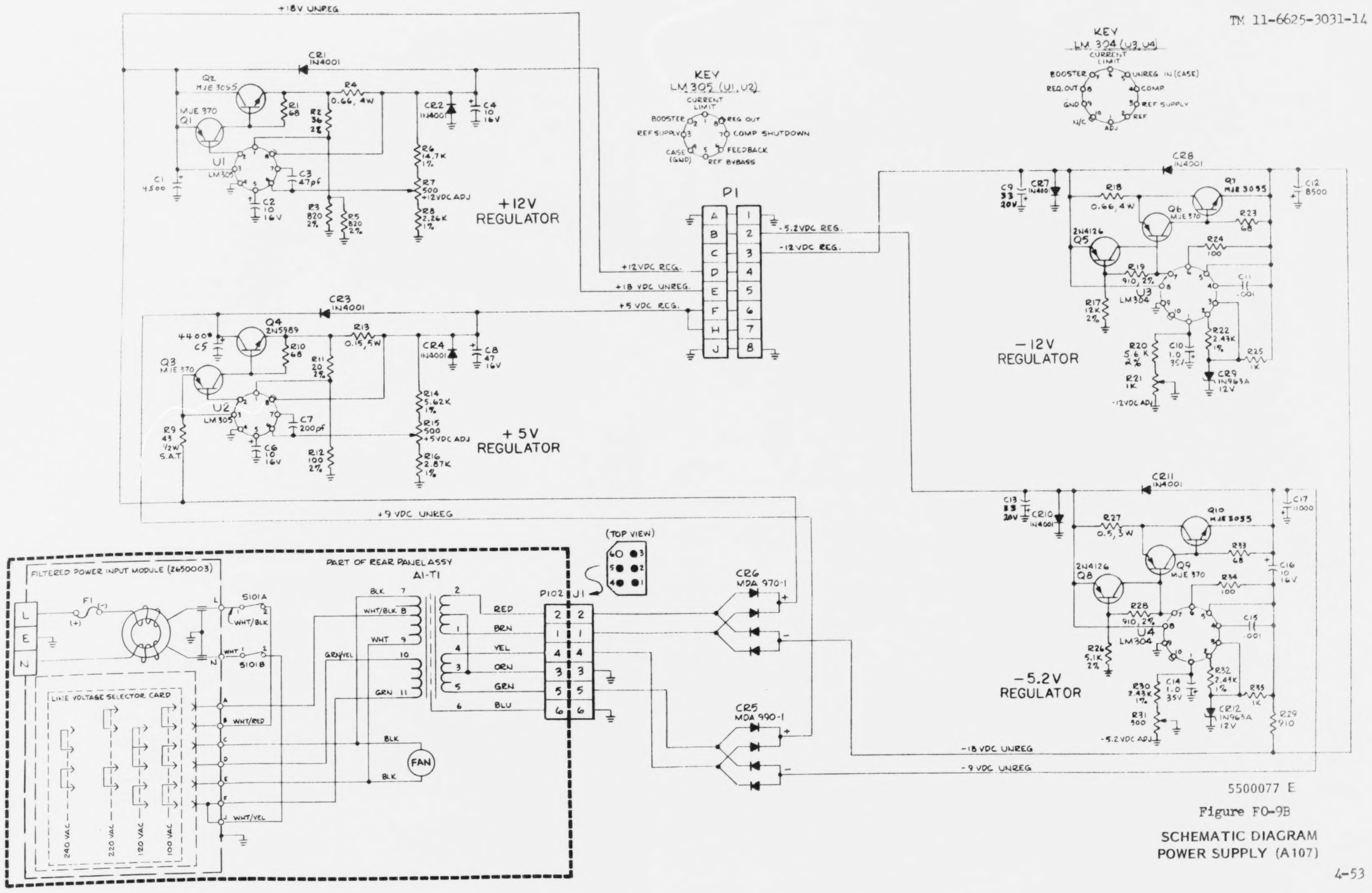
All the regulated voltages are produced by full wave rectifier and series regulator circuits. The +18 V unregulated voltage is also the input voltage for the +12 V regulator.

Each of the four regulator circuits contains an integrated circuit voltage regulator with current foldback capability, protective diodes, and provision for adjustment of the required output voltage.

The type of IC used in both the +12 V and +5 V regulators is an LM 305. This IC contains an internal temperature compensated voltage reference, as well as the necessary circuits to provide gain and current foldback limiting. The foldback current limit control resistors in the +5 V supply (for example), are R11, R12, and R13.

The negative supplies utilize an LM 304 as the basic IC regulator. This IC also contains an internal temperature compensated reference. To implement this reference an external pre-regulator is required. In the -12 V circuit (for example), the pre-regulator includes R22, R25, and CR9. Current foldback limiting uses internal IC circuitry in addition to R17, R18, R19 and Q5.

Figure FO-9A
Component Locator
and
Descriptive Information
POWER SUPPLY (A107)


+18V UNREG
CR1 1N4001
Q2 MJE3055
Q1 MJE370
U1 LM305
R4 0.66, 4W
CR2 1N4001
C4 10 16V
C1 4500
C3 47pf
C2 10 16V
R6 14.7K 1%
R7 500 +12VDC ADJ
R8 2.26K 1%
+12V REGULATOR
KEY
LM 305 (U1, U2)
CURRENT LIMIT
BOOSTER
REG OUT
REF SUPPLY
COMP SHUTDOWN
CASE (GND)
FEEDBACK
REF BYPASS
P1
+12VDC REG.
+18 VDC UNREG.
+5 VDC REG.
-5.2VDC REG.
-12 VDC REG.
CR3 1N4001
Q4 2N5989
Q3 MJE370
C5 4400
U2 LM305
R13 0.15, 5W
CR4 1N4001
C8 47 16V
C7 200pf
C6 10 16V
R9 S.A.T.
R14 5.62K 1%
R15 500 +5VDC ADJ
R16 2.87K 1%
+5V REGULATOR
+9 VDC UNREG
KEY
LM 304 (U3, U4)
CURRENT LIMIT
BOOSTER
UNREG IN (CASE)
REG OUT
COMP
GND
REF SUPPLY
N/C
ADJ
REF
CR8 1N4001
C9 33 20V
CR7 1N4001
R18 0.66, 4W
Q7 MJE3055
Q6 MJE370
C12 8500
Q5 2N4126
U3 LM304
-12V REGULATOR
CR9 1N963A 12V
-12VDC ADJ
CR11 1N4001
C13 33 20V
CR10 1N4001
R27 0.5, 5W
Q10 MJE3055
Q9 MJE370
C17 11000
C16 10 16V
Q8 2N4126
U4 LM304
-5.2V REGULATOR
CR12 1N963A 12V
-5.2VDC ADJ
R29 910
-18 VDC UNREG
-9 VDC UNREG
PART OF REAR PANEL ASSY
A1-T1
FILTERED POWER INPUT MODULE (2650003)
L
E
N
F1
S101A
S101B
WHT/BLK
WHT/RED
WHT/YEL
LINE VOLTAGE SELECTOR CARD
240 VAC
220 VAC
120 VAC
100 VAC
BLK
WHT
GRN/YEL
GRN
FAN
RED
BRN
YEL
ORN
GRN
BLU
P102
J1
(TOP VIEW)
CR6 MDA 970-1
CR5 MDA 990-1

5500077 E

Figure FO-9B

SCHEMATIC DIAGRAM
POWER SUPPLY (A107)

## REFERENCE OSCILLATOR BUFFER (A108)

### GENERAL

A room temperature, crystal controlled oscillator (RTO) is used as the basic reference against which all input signals are compared. An additional temperature-compensated crystal oscillator (TCXO) is available as Option P1, which allows the user to select a higher level of precision compatible with measurement requirements.

### Circuit Description

The signal from the oscillator is either a square wave from the RTO, or a sine wave from the optional TCXO. This waveform is converted to a positive-going square wave at J1 by a linear amplifier (Q1), current switch (Q2,Q3), and an output current driver (Q4).

The outputs appearing at P1 pins 6 and 14,are processed by a linear, low gain amplifier pair (Q5 and Q6), and two identical line driver circuits Q7-Q10, and Q11-Q14). Low gain, common emitter input stages (Q7,Q11), are followed by emitter followers (Q8, Q12), which drive push-pull emitter follower output pairs (Q9,Q10, and Q13,Q14).

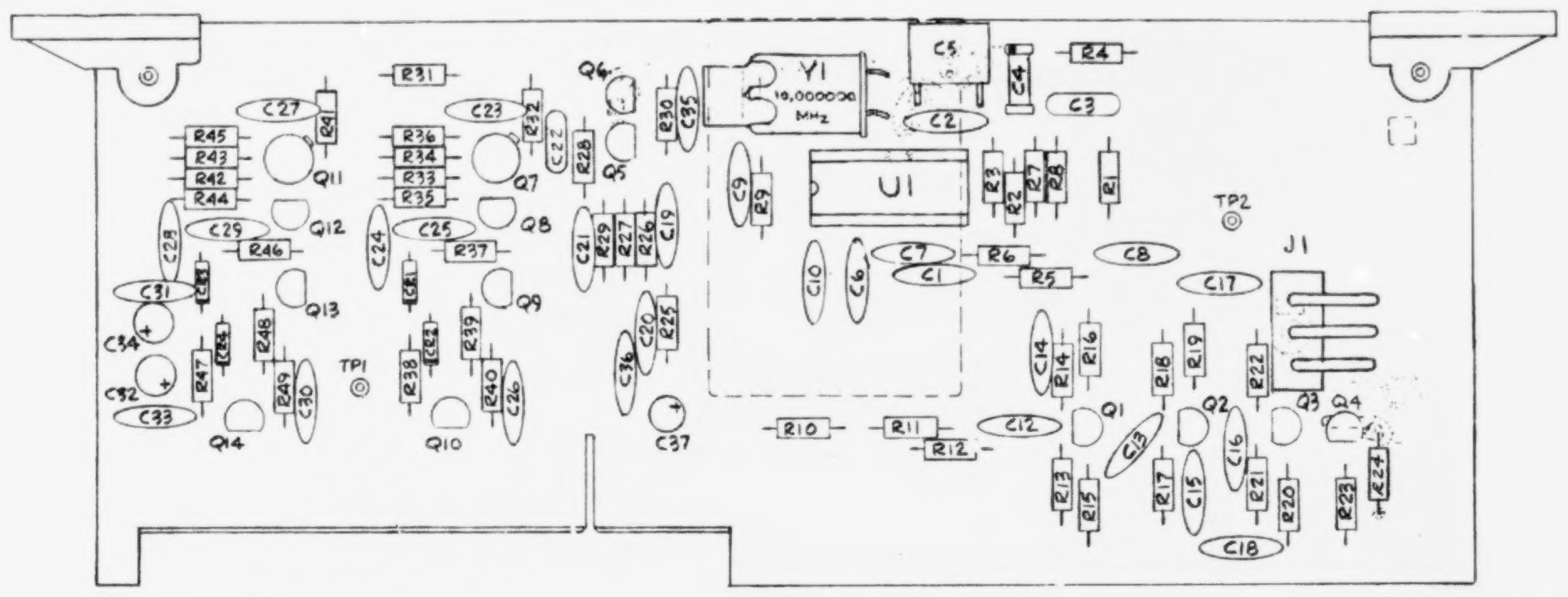
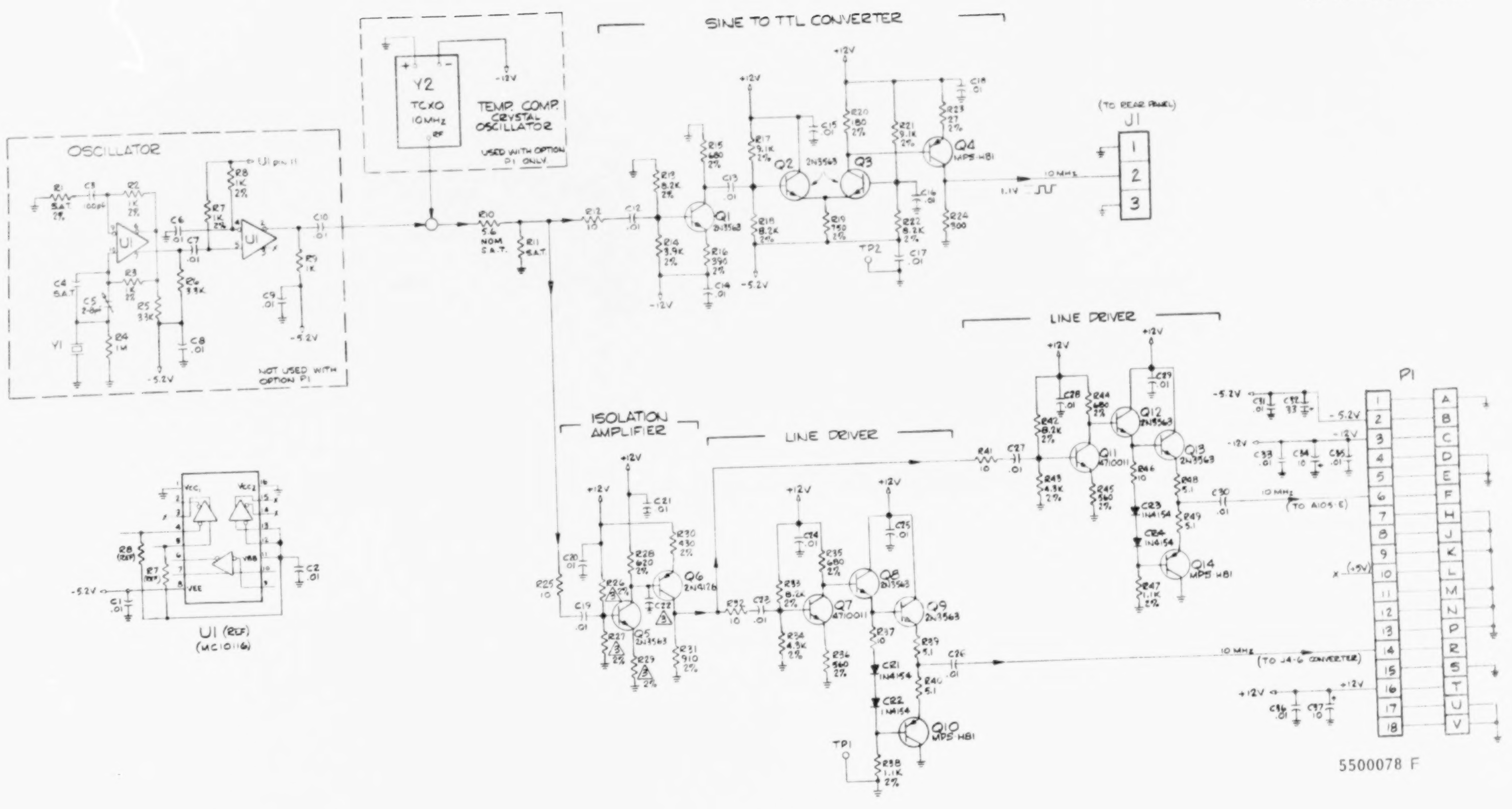

R31
C27
R41
C23
R32
Q6
R30
C35
Y1
10,000000 MHz
C5
C4
R4
C3
C2
R45
R43
R42
R44
Q11
R36
R34
R33
R35
Q7
C22
R28
Q5
C9
R9
U1
R3
R2
R7
R8
R1
TP2
C28
C29
Q12
R46
C24
C25
Q8
R37
C21
R29
R27
R26
C19
C7
C1
R6
R5
C8
J1
C17
C31
Q13
Q9
C10
C6
C34
C32
C33
R47
R48
R49
C30
TP1
R38
R39
R40
C26
C20
R25
C36
C37
Q14
Q10
C14
R14
R16
R18
R19
R22
Q1
Q2
Q3
Q4
R10
R11
R12
C12
C13
C16
R13
R15
R17
C15
R21
R20
R23
R24
C18
2020078 L

Figure FO-10A
Component Locator
and
Descriptive Information
REFERENCE OSCILLATOR BUFFER (A108)

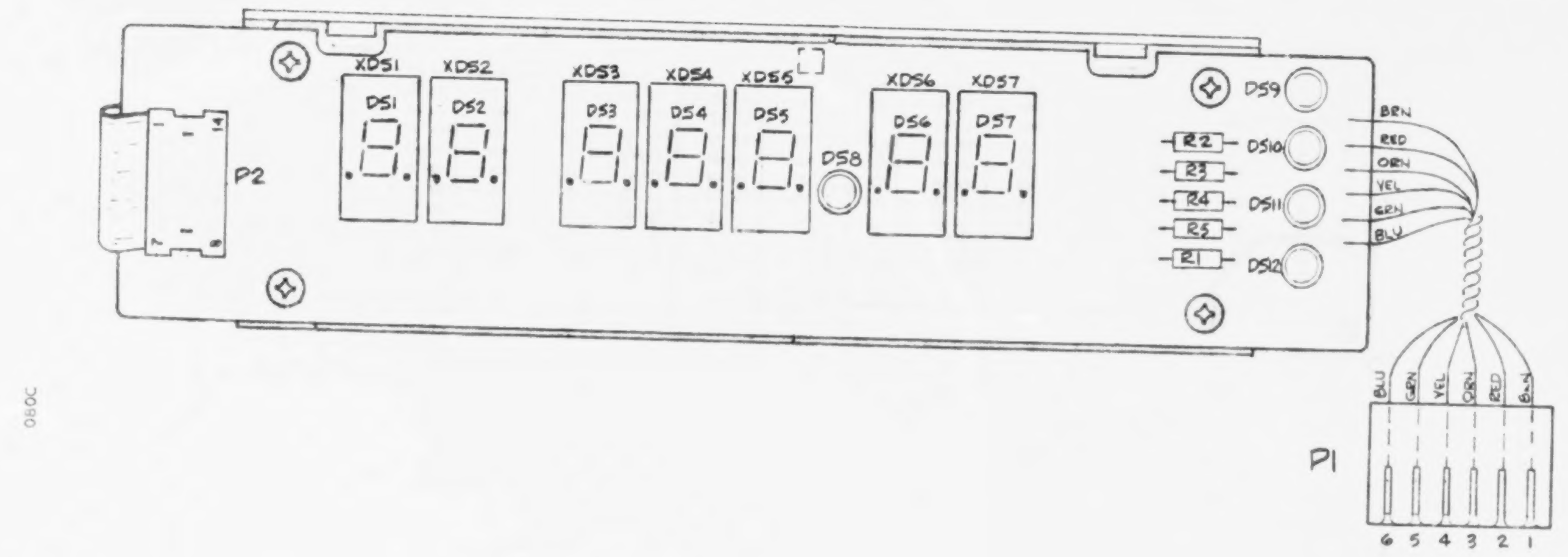

OSCILLATOR
NOT USED WITH OPTION P1
Y2
TCXO
10MHz
TEMP COMP CRYSTAL OSCILLATOR
USED WITH OPTION P1 ONLY
SINE TO TTL CONVERTER
(TO REAR PANEL)
J1
1
2
3
ISOLATION AMPLIFIER
LINE DRIVER
LINE DRIVER
P1
U1 (REF)
(MC10116)
TP1
TP2
-5.2V
+12V
-12V
10 MHz
(TO A105-E)
(TO 14-6 CONVERTER)
5500078 F

| REF DESIG. | STD (RM TEMP OSC) | OPT P1 (TCXO) |
|---|---|---|
| R26 | 11K | 9.1K |
| R27 | 1.3K | 2.2K |
| R29 | 100 | 360 |
| C22 | 33pf. S.A.T. | NOT USED |
| | | |

△3 COMPONENT VALUES CHANGE WHEN TCXO OPTION P1 IS USED. SEE TABLE FOR CORRECT COMPONENT VALUE FOR EACH APPLICATION.

Figure FO-10B

SCHEMATIC DIAGRAM
REFERENCE OSCILLATOR BUFFER (A108)



## DISPLAY (A110)

Display board A110 contains seven LED numerical display units mounted side-by-side, grouped into a 2-digit GHz section, and a 5-digit MHz section. The MHz section also contains an LED decimal point between the second and third least-significant-digits (decimal point extinguishes when the two least-significant-digits are blanked by the front panel RESOLUTION switches). All drive signals for the display are obtained from the Count Chain Control.

The digit displays are 7-segment LED's, with the anodes of all segments of each digit tied together. When the anode is at a positive voltage, grounding any cathode through its associated resistor illuminates that segment.

In this multiplexed system, the anode supply voltage is applied in pulses (through anode drivers), which are synchronized with the cathode data to determine which segment shall light. The segment drive is applied directly to all display digits. Corresponding cathode segments are all tied together in groups of seven.

The LED digits each use a single transistor driver. The drivers saturate when turned on, applying a voltage almost equal to the supply voltage for the display. This voltage is variable (by A102R35) for display brightness adjustment.

Four display lamps are included on this assembly, which illuminate to indicate GATE operation, input signal LEVEL, LOCK, and REMOTE operation (Option P4).

Figure FO-11A
Component Locator
and
Descriptive Information
DISPLAY (A110)

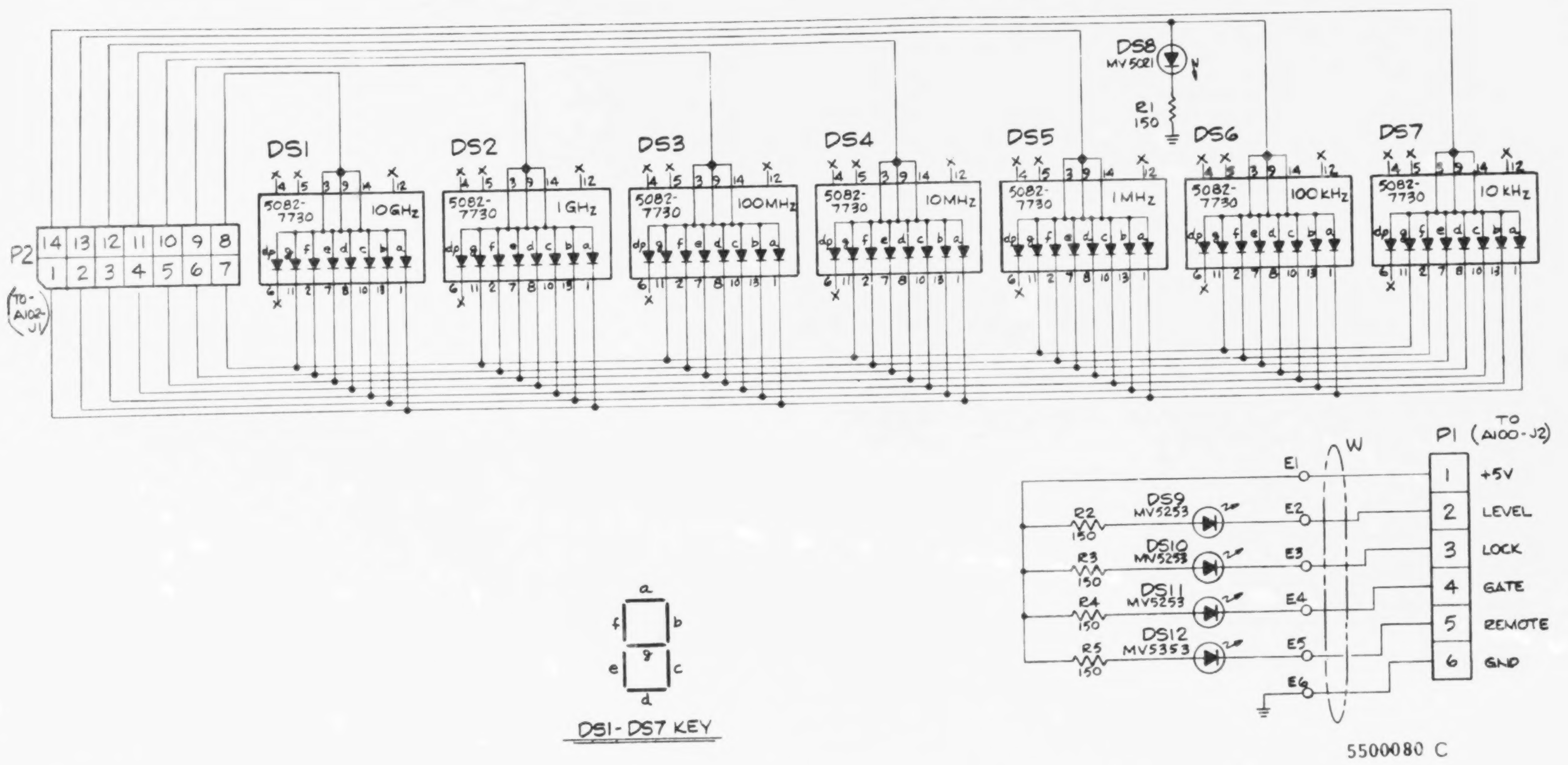

P2
(TO-A102-J1)
14 13 12 11 10 9 8
1 2 3 4 5 6 7
DS1
5082-7730
10GHz
DS2
5082-7730
1GHz
DS3
5082-7730
100MHz
DS4
5082-7730
10MHz
DS5
5082-7730
1MHz
DS6
5082-7730
100kHz
DS7
5082-7730
10kHz
dp g f e d c b a
DS8
MV5021
R1
150
P1 (TO A100-J2)
W
E1
E2
E3
E4
E5
E6
DS9
MV5253
DS10
MV5253
DS11
MV5253
DS12
MV5353
R2
150
R3
150
R4
150
R5
150
1 +5V
2 LEVEL
3 LOCK
4 GATE
5 REMOTE
6 GND
a b c d e f g
DS1-DS7 KEY
5500080 C

Figure FO-11B
SCHEMATIC DIAGRAM
DISPLAY (A110)

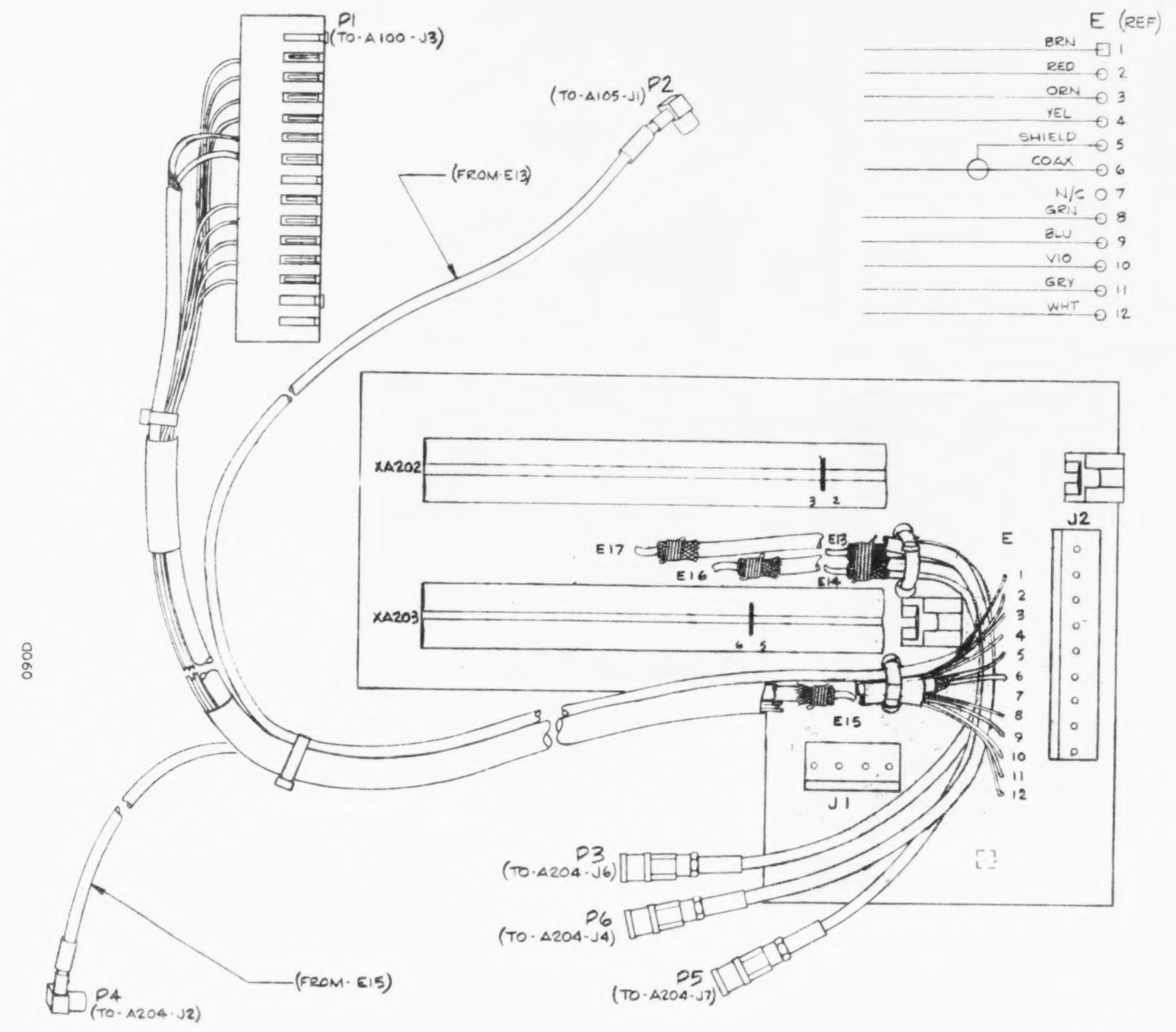

P1
(TO-A100-J3)
(TO-A105-J1) P2
(FROM-E13)
E (REF)
BRN 1
RED 2
ORN 3
YEL 4
SHIELD 5
COAX 6
N/C 7
GRN 8
BLU 9
VIO 10
GRY 11
WHT 12
XA202
3 2
E17
E16
E13
E14
E
J2
XA203
6 5
1
2
3
4
5
6
7
8
9
10
11
12
E15
J1
090D
P3
(TO-A204-J6)
P6
(TO-A204-J4)
P5
(TO-A204-J7)
(FROM-E15)
P4
(TO-A204-J2)

Figure FO-12A
COMPONENT LOCATOR
CONVERTER INTERCONNECT (A200)

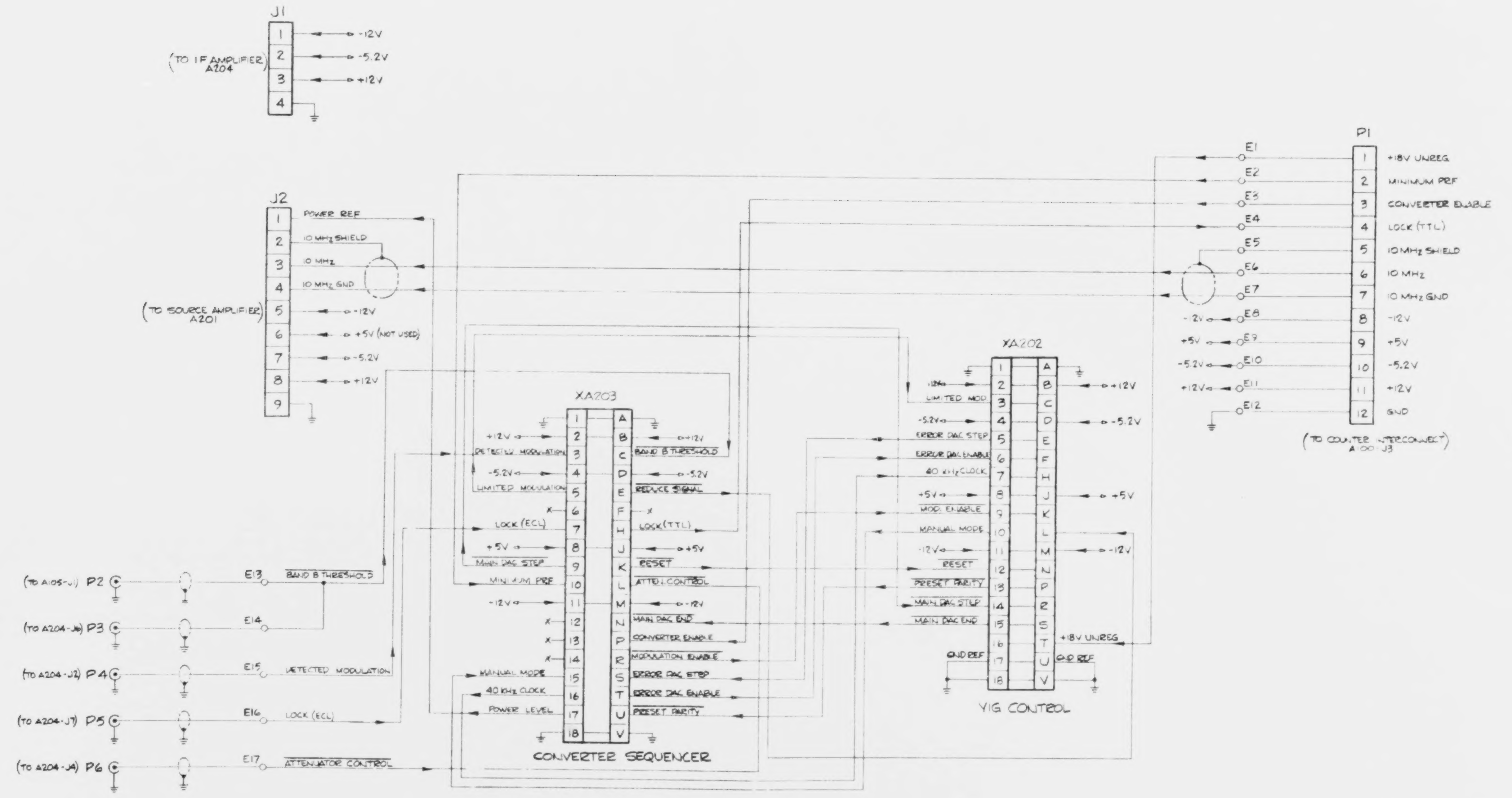
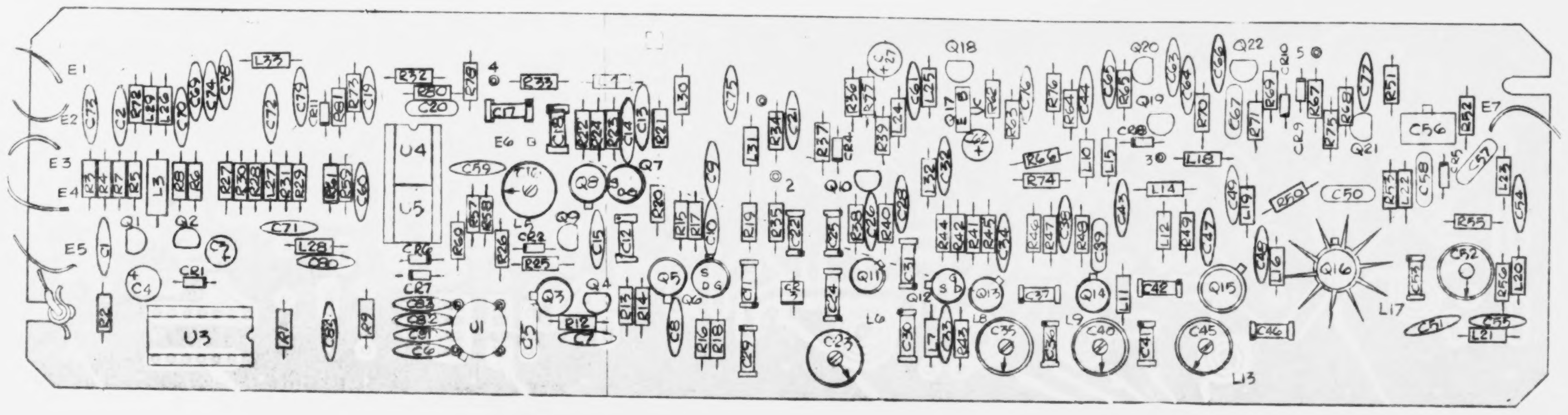

J1
(TO IF AMPLIFIER A204)
1 -12V
2 -5.2V
3 +12V
4
J2
(TO SOURCE AMPLIFIER A201)
1 POWER REF
2 10 MHz SHIELD
3 10 MHz
4 10 MHz GND
5 -12V
6 +5V (NOT USED)
7 -5.2V
8 +12V
9
XA203
1 A
2 +12V B +12V
3 DETECTED MODULATION C BAND B THRESHOLD
4 -5.2V D -5.2V
5 LIMITED MODULATION E REDUCE SIGNAL
6 F
7 LOCK (ECL) H LOCK (TTL)
8 +5V J +5V
9 MAIN DAC STEP K RESET
10 MINIMUM PRF L ATTEN CONTROL
11 -12V M -12V
12 N MAIN DAC END
13 P CONVERTER ENABLE
14 R MODULATION ENABLE
15 MANUAL MODE S ERROR DAC STEP
16 40 KHz CLOCK T ERROR DAC ENABLE
17 POWER LEVEL U PRESET PARITY
18 V
CONVERTER SEQUENCER
XA202
1 A
2 +12V B +12V
3 LIMITED MOD C
4 -5.2V D -5.2V
5 ERROR DAC STEP E
6 ERROR DAC ENABLE F
7 40 KHz CLOCK H
8 +5V J +5V
9 MOD. ENABLE K
10 MANUAL MODE L
11 -12V M -12V
12 RESET N
13 PRESET PARITY P
14 MAIN DAC STEP R
15 MAIN DAC END S
16 T +18V UNREG
17 GND REF U GND REF
18 V
YIG CONTROL
P1
E1 1 +18V UNREG
E2 2 MINIMUM PRF
E3 3 CONVERTER ENABLE
E4 4 LOCK (TTL)
E5 5 10 MHz SHIELD
E6 6 10 MHz
E7 7 10 MHz GND
-12V E8 8 -12V
+5V E9 9 +5V
-5.2V E10 10 -5.2V
+12V E11 11 +12V
E12 12 GND
(TO COUNTER INTERCONNECT A100-J3)
(TO A105-J1) P2 E13 BAND B THRESHOLD
(TO A204-J6) P3 E14
(TO A204-J2) P4 E15 DETECTED MODULATION
(TO A204-J7) P5 E16 LOCK (ECL)
(TO A204-J4) P6 E17 ATTENUATOR CONTROL
090A

Figure FO-12B

SCHEMATIC DIAGRAM
CONVERTER INTERCONNECT (A200)



2020091 U

## SOURCE AMPLIFIER (A201)

### General

A source of up to one watt of power at 200 MHz is required to drive the step recovery diode Comb Generator in YIG Assembly A207. The 200 MHz must be both stable and coherent with the master oscillator in the counter. Stability is required to provide an IF spectrum that is dependent only upon the input signal spectrum. Coherence with the master oscillator is required to make counting accuracy dependent only upon the accuracy of the master oscillator.

The requirements of stability and coherence are satisfied by using a phase locked loop to lock a 200 MHz LC oscillator to the 10 MHz time base oscillator. The required output power is generated by a Class C amplifier that contains a leveling loop to set the power output at any desired level from 1 mW to 1.1 W.

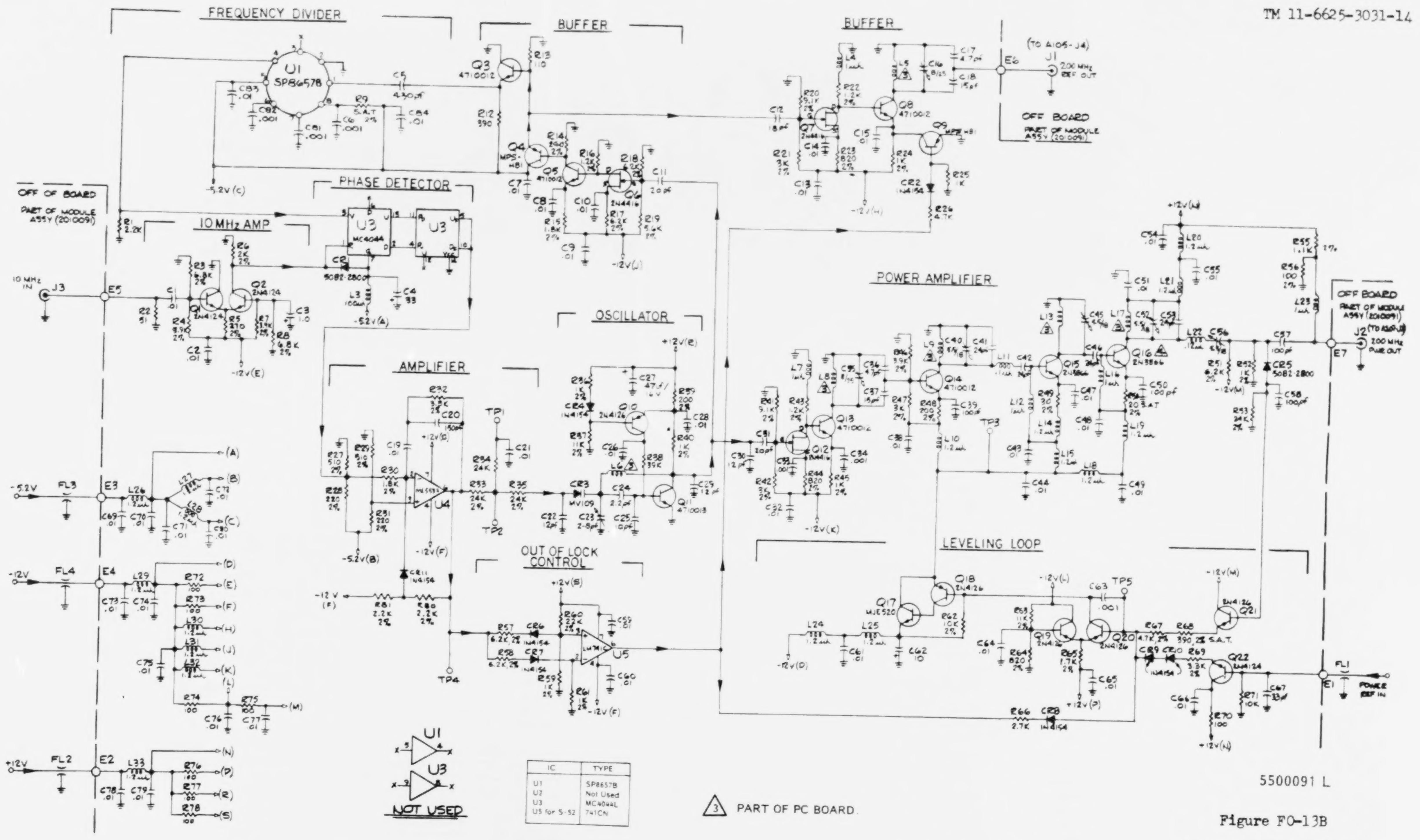
### Circuit Description

The phase lock loop is a standard second order loop, implemented by using digital phase lock loop components. The 200 MHz LC oscillator is a modified Colpitts circuit with bias stabilization supplied by Q10. The output frequency of the 200 MHz oscillator is divided by 20 in U1 and U2 to produce a 10 MHz square wave. This signal is compared to the processed 10 MHz reference by phase detector U3. Phase error is amplified by active filter U4,and applied to voltage variable capacitor CR3. This holds the 200 MHz oscillator "locked" in phase to the 10 MHz reference signal. C23 sets the open loop center frequency of the oscillator.

The main power amplifier consists of four stages: buffer amplifier Q12 and Q13, linear amplifier Q14, and two Class C stages Q15 and Q16. Output power level is controlled by adjusting the value of the negative voltage supplied by Q17 and Q18 to the linear amplifier and Class C stages.

The power leveling loop operates by sampling the peak value of the output signal with CR5, and comparing this peak value to the Power Reference. The comparison is made by differential amplifier Q19 and Q20, which in turn controls Q17 and Q18.

Figure FO-13A
Component Locator
and
Descriptive Information
SOURCE/AMPLIFIER (A201)


FREQUENCY DIVIDER
BUFFER
BUFFER
U1
SP8657B
PHASE DETECTOR
U3
MC4044
10 MHz AMP
OFF OF BOARD
PART OF MODULE A55Y (20.00%)
10 MHz IN
J3
E5
OSCILLATOR
AMPLIFIER
U4
OUT OF LOCK CONTROL
U5
TP1
TP2
TP3
TP4
TP5
POWER AMPLIFIER
LEVELING LOOP
(TO A105-J4)
J1
E6
200 MHz REF OUT
OFF BOARD
PART OF MODULE A55Y (20.00%)
OFF BOARD
J2
E7
200 MHz PWR OUT
FL1
E1
POWER REF IN
-52V
FL3
E3
-12V
FL4
E4
+12V
FL2
E2
NOT USED

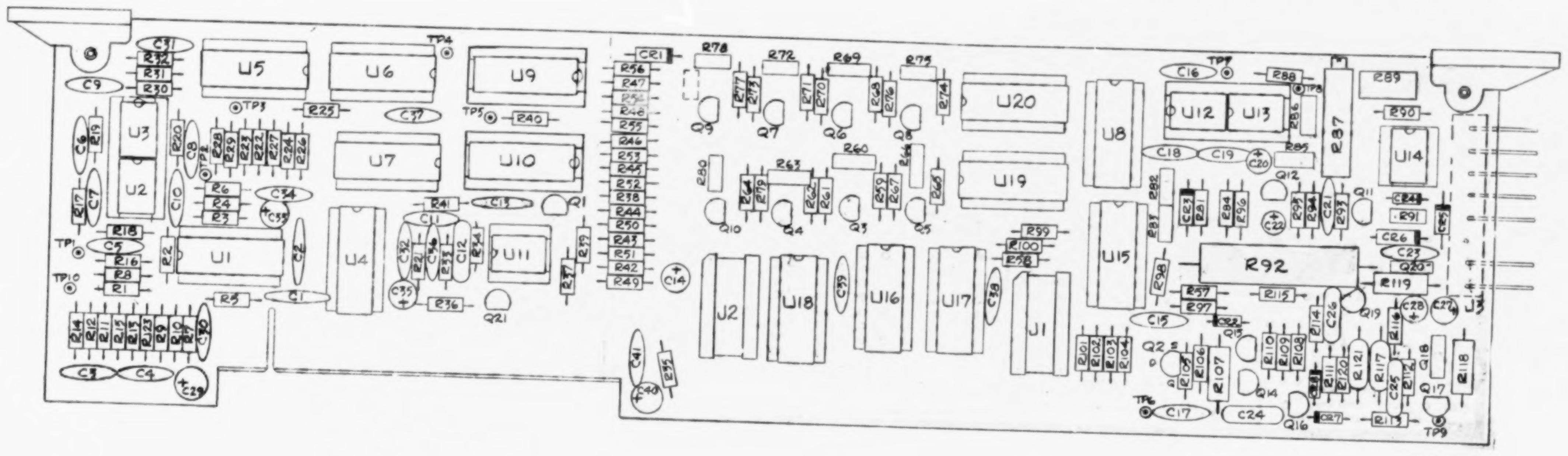
| IC | TYPE |
|---|---|
| U1 | SP8657B |
| U2 | Not Used |
| U3 | MC4044L |
| U5 for S-52 | 741CN |

△3 PART OF PC BOARD.

5500091 L

Figure FO-13B

SCHEMATIC DIAGRAM
SOURCE/AMPLIFIER (A201)



2020092 P

## YIG CONTROL (A202)

### General

The YIG Control Board (A202) contains circuits required to set the frequency of the YIG filter (A207) and to generate the BCD preset information for the Count Chain (A103). The main digital-to-analog converter (DAC) selects a particular comb line and provides the output frequency information. An error DAC provides a correction signal to precisely center the YIG filter passband on a comb line, based on information derived from the centering circuits. These circuits operate by modulating the center frequency of the YIG passband at a 20 kHz rate. This causes the filter to be tuned back and forth through the desired comb line, producing a pulse each time the YIG passes through the comb frequency. The phase of this detected modulation is then compared to the modulation frequency to produce the required centering information.

### Main DAC

Steps of 200 MHz to the YIG filter are controlled by the main DAC. This DAC consists of a voltage reference (CR3, U12), presettable BCD counters (U19, U20), a series of transistor switches (Q3-Q10), precision summing resistors, and a summing amplifier (U13). Data from the front panel thumbwheel switch is preset into U19 and U20 during the Reset period. Each output line controls a transistor switch which connects a precision resistor to the 3.1V voltage reference. The value of the resistor determines the current into the SUM line, while the summing amplifier provides a voltage output proportional to the total input current. The digital output of U19 and U20 are also used to provide 3MSD preset information to A103.

In the AUTO mode, pulses from A203 into the clock input of U19 cause the DAC to step in 200 MHz increments upon command. In the MANUAL mode, a Parity Checker (U16, U17, U18), compares the thumbwheel information with the actual states of U19 and U20. If they differ, an output is obtained which triggers a Reset, and in turn causes the DAC output to equal the thumbwheel switch setting.

### YIG Driver

The voltage output of the summing amplifier is converted into a current in the YIG Driver (U14, Q11, Q12, and chassis mounted A2Q1). R89 sets the current offset, while R87 sets the slope. The current sense resistor (R92) provides the required feedback voltage for the driver. CR5 limits the voltage across the YIG filter tuning coil during Reset in order to protect Q12 and A2Q1.

### YIG Passband Modulation

As part of the centering function, the center frequency of the YIG passband is modulated by means of an auxiliary tuning coil within the YIG. A 40 kHz clock is divided in U4 to produce a 20 kHz square wave. This signal is converted to a triangular waveform by integrator U11. This output is then converted to a current in the Modulation Coil Driver. Q14-Q16 form a high gain voltage amplifier. The single ended output at the collector of Q16 is converted to a bipolar output with Q17 and Q19, while CR7 and CR8 compensate for base emitter junction voltages. Q18 and Q20 provide increased current capability. Feedback for the driver is supplied by sensing the current through R107, thus converting the voltage input to a current output. Nominal deviation of the YIG center frequency is ± 50 MHz.

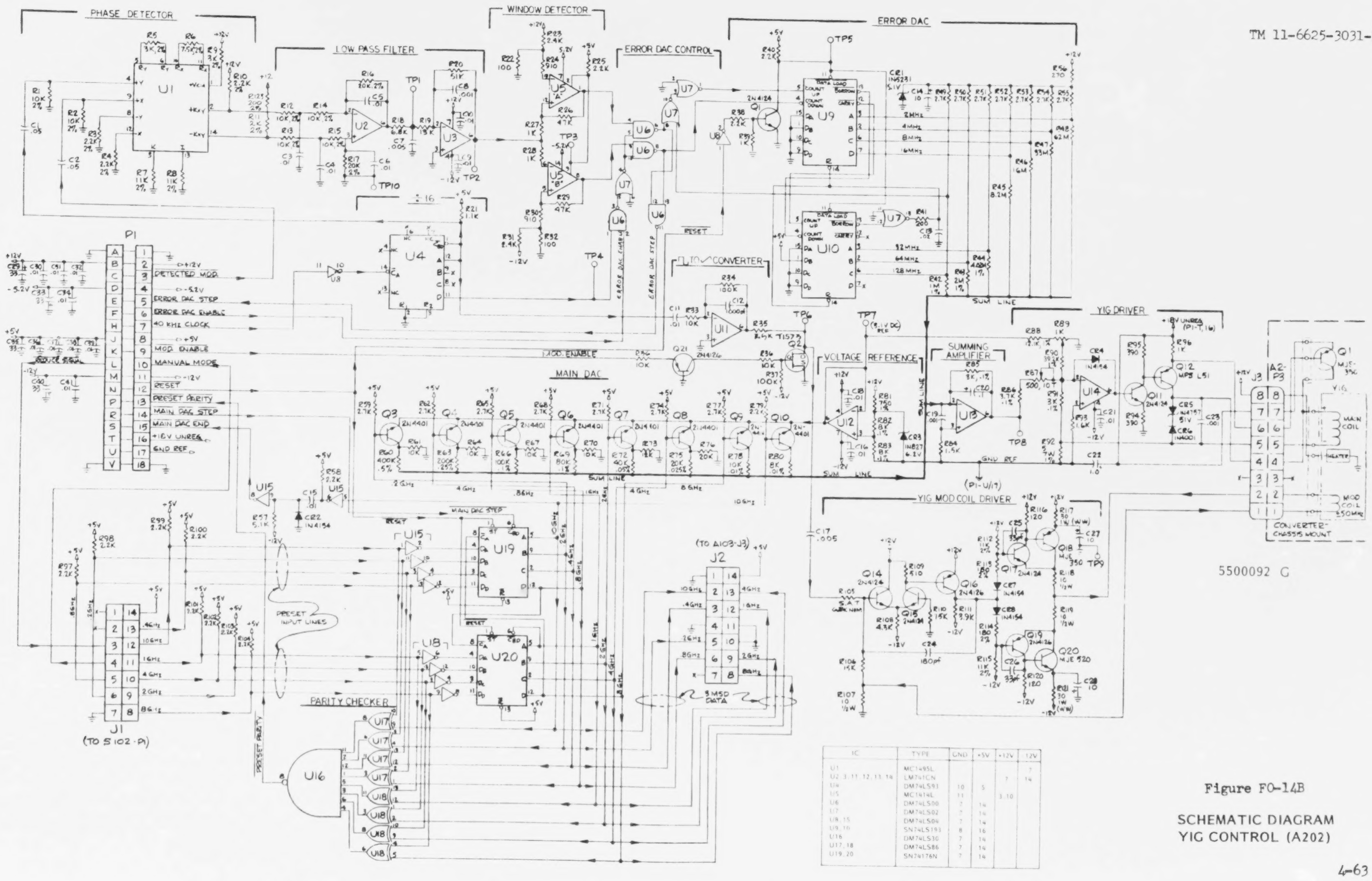
### YIG Centering Circuit

Centering of the YIG passband is achieved by detecting the output of the modulated comb generator and phase comparing it to the modulation frequency in U1. U1 is a four quadrant multiplier, producing outputs proportional to the product of two inputs. The positive and negative outputs of U1 differentially drive an active low pass filter (U2), which in turn, drives another low pass filter (U3). The output of U3 represents the DC component of the output of U1. Its amplitude and sign are directly related to the frequency offset of the YIG filter passband from the comb frequency. This signal is sensed by window detector U5. If the output at U3 exceeds the threshold reference, one of the two outputs of U5 is driven high.

The two outputs of U5 are used to control the Error DAC. This DAC supplies an error signal directly into the Main DAC summing amplifier. R42-R48 are summing resistors switched on by U9 and U10 (binary up-down counters). Clock pulses from U4 at a 2.5 kHz rate cause U9 to either count up, count down, or remain fixed depending on the outputs of U5.

Thus, a continually increasing (or decreasing) error signal is applied to the main tuning coil of the YIG until the DC output of U3 falls inside the threshold limits. The Borrow output of U10 provides a low level clamp on the DAC, while the C output of U10 provides a high level clamp. The Error DAC step at U6 pin 11 provides the information to the Converter Sequencer (A203) that the YIG centering cycle is completed.

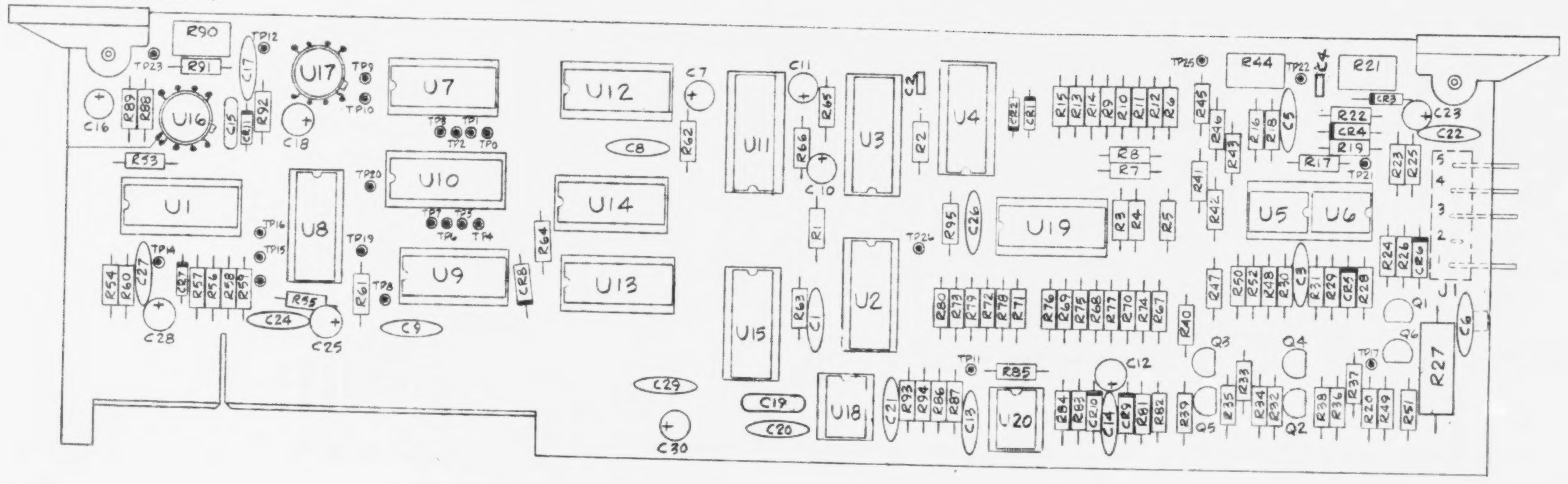
Figure FO-14A
Component Locator
and
Descriptive Information
YIG CONTROL (A202)


PHASE DETECTOR
LOW PASS FILTER
WINDOW DETECTOR
ERROR DAC CONTROL
ERROR DAC
TP5
U1
U2
U3
U4
U9
U10
TP1
TP2
TP3
TP4
TP10
÷16
P1
DETECTED MOD
ERROR DAC STEP
ERROR DAC ENABLE
40 KHz CLOCK
MOD ENABLE
MANUAL MODE
RESET
PRESET PARITY
MAIN DAC STEP
MAIN DAC END
+15V UNREG
GND REF
I/V CONVERTER
VOLTAGE REFERENCE
SUMMING AMPLIFIER
YIG DRIVER
MAIN DAC
YIG MOD COIL DRIVER
MAIN COIL
MOD COIL
CONVERTER CHASSIS MOUNT
J1
(TO 5102-P1)
J2
(TO A103-J3)
PRESET INPUT LINES
PARITY CHECKER
U16
U19
U20
5500092 G

| IC | TYPE | GND | +5V | +12V | -12V |
|---|---|---|---|---|---|
| U1 | MC1495L | | | | 7 |
| U2,3,11,12,13,14 | LM741CN | | | 7 | 14 |
| U4 | DM74LS93 | 10 | 5 | | |
| U5 | MC1414L | 11 | | 3,10 | |
| U6 | DM74LS00 | 7 | 14 | | |
| U7 | DM74LS02 | 7 | 14 | | |
| U8,15 | DM74LS04 | 7 | 14 | | |
| U9,10 | SN74LS193 | 8 | 16 | | |
| U16 | DM74LS30 | 7 | 14 | | |
| U17,18 | DM74LS86 | 7 | 14 | | |
| U19,20 | SN74176N | 7 | 14 | | |

**Figure FO-14B**

SCHEMATIC DIAGRAM
YIG CONTROL (A202)



## CONVERTER SEQUENCER (A203)

### General

The Converter Sequencer (A203) generates the signals required to step the RF Converter (A2) through its specified frequencies. The board contains a Sequence Generator to generate properly timed start and stop commands for all the required functions. Among the circuits controlled are: the attenuator control and driver circuitry for leveling and switching of the incoming signal, the power level control circuit for controlling the YIG comb power, and Error DAC (digital-to-analog converter) signals controlling the timing of the YIG filter centering circuitry.

### Sequence Generator

The basic part of the Converter Sequencer is the Sequence Generator, composed of a binary counter (U8) and a demultiplexer (U10). This circuit generates eight discrete steps, each of which is identified by a low on a corresponding test point (TP0 - TP7).

U8 is driven by a 40 kHz clock (U18) through a network of gates which allow holding the Sequence Generator in any given step until a set of specific conditions signifies that the step is completed. The function of each sequence is shown in Table 4-7.

Sequence 0 is the state the converter sequence goes to when the converter is disabled. Sequence 0 sets a latch (U12 pin 1) whose output turns off the RF signal by setting the attenuator driver to maximum attenuation, and sending a command to the YIG Control board (A202) to begin the 20 kHz YIG coil modulation. Sequence 0 also sends out a Main DAC step command which steps the Main DAC to the next comb line unless the Converter is being disabled. If so, the disable reset command over-rides the DAC step, and the YIG stops at the bottom (or preset) frequency.

Sequence 1 begins the YIG power leveling cycle. A 1.5 ms one-shot (U11) resets the YIG power DAC (U19) for minimum power, and sets a latch (U15 pins 3,8), whose output inhibits the clock into the Sequence Generator until the power leveling cycle is complete. At the end of the 1.5 ms reset time, the YIG power DAC begins increasing the LO power into the Mixer until either the detected modulation (P1 pin 3) exceeds its threshold, or the LO power reaches its maximum output. At this point the U15 latch is reset which stops the clocking of the power DAC and allows the Sequence Generator to move to the next step.

Sequence 2 begins the YIG coil centering cycle. The centering circuitry is located on the YIG Control board (A202), but the enable time is controlled by the Converter Sequencer.

A 1 ms one-shot is triggered by Sequence 2. Two outputs are taken from the one-shot: the Q output which is used as an Error DAC enable signal to turn on the centering circuitry on the YIG Control board; and $\overline{Q}$ output which is fed back to hold the Sequence Generator in Sequence 3 until the centering process is completed. The end of this process is indicated by a lack of error DAC step pulses. When this occurs, the one-shot times out, and the Sequence Generator is released to go on to Sequence 4.

Sequence 4 is the first step of the sequence in which the input signal is examined. In this step, the latch (U12 pin 1) controlling the input signal is reset; this also turns off the YIG modulation. A second latch (U12 pin 12) is set at the start of Sequence 4. This latch inhibits the sequence during Sequence 5 until a Band B Threshold signal is obtained. This step thus guarantees that at least one input signal has been received during either Sequence 4 or 5.

Sequence 6 is used as a 25 µ sec delay period to provide the necessary time for operation of the Attenuator Control on signals with slow rise times. This is discussed further in the Attenuator Control paragraphs below.

Sequence 7 is the LOCK sensing portion of the sequence. If the signal received during Sequence 4 or 5 resulted in a LOCK command from the IF Processor, then the sequence will remain in Sequence 7, and send a LOCK command to the Control board (A104) in the Basic Counter. If no LOCK was obtained, the Sequencer will continue to Sequence 0, and repeat the sequence with the next comb line.

### Attenuator Control

The Attenuator Control circuits perform the function of limiting the variations in input signal amplitude as seen by the Mixer (A205). The ATTENUATOR CONTROL command from the IF Processor (A204) is activated whenever the input signal received by A205 exceeds the minimum signal by at least 7 dB. This command triggers one-shot U3. The output of U3 drives a DAC consisting of a counter (U4), summing resistors (R9 - R14), a summing amplifier (U5), and an inverting amplifier (U6). Each DAC step results in a nominal 0.5 dB increase in attenuator insertion loss. The REDUCE SIGNAL indicator on the front panel is activated when the DAC reaches its 32nd step.

The DAC acts as a sample and hold circuit for attenuation level. As long as there is insufficient attenuation, the ATTENUATOR CONTROL command will cause the attenuation to increase 0.5 dB for each input pulse. On long pulses or CW signals, U3 will retrigger as long as the ATTENUATOR CONTROL command remains active.

In addition to increasing attenuator insertion loss, the ATTENUATOR CONTROL command forces the Sequence Generator to Sequence 3 by activating the preset strobe line of U8. Since the RF switch remains open, and the YIG modulation is not enabled, the Sequencer then moves on through Sequence 4 and 5, and again waits for Band B Threshold. The result is that the Sequencer cannot go on to Sequence 6 until the attenuator has reduced the input signal sufficiently.

### Attenuator Driver

The output of U6 is a voltage corresponding to the desired attenuation. This signal is converted into two related currents by the Attenuator Driver. These currents: $I_{total}$ and $I_{series}$, determine both the attenuation and the input VSWR of the PIN Diode Attenuator (part of A206).

Series current is generated by the network of U5 and Q6. R53 is the sense resistor for the current source. The nonlinear current output versus input level is achieved with a double breakpoint shaping network — Q2 and Q3 form one breakpoint, while Q4 and Q5 form the other. Variable resistor R47 sets the series current, and optimizes VSWR, at high attenuation levels.

Total current is the sum of series current and shunt current. The shunt current waveform is shaped by diode network CR2, CR3, and their associated resistors. Variable resistor R23 is used to adjust the ratio between series and shunt currents at moderate attenuation levels. U6 and current booster Q1, combine series and shunt networks to produce the total current output.

### Power Level Control

During Sequence 1, the YIG comb level is set. This function is accomplished by varying the POWER REFERENCE level into the Source/Amplifier (A201). This in turn varies the 200 MHz power into the YIG/Comb Generator (A207). The comb line output is detected by the Mixer, and sensed by the Threshold Detector U17. Variable resistor R64 sets the threshold level.

Operation of the Power Level Control begins at the end of the 1.5 ms period of U11. Clock pulses from U18 are then allowed to step the Power Level DAC (U19, R74 thru R80). When the comb output exceeds the threshold, U17 triggers, resetting the latch (U15 pin 10), inhibiting the clock input to the DAC and ending the sequence. If the DAC reaches maximum output, the same result is obtained.

Figure FO-15A

Component Locator
and
Descriptive Information
CONVERTER SEQUENCER (A203)

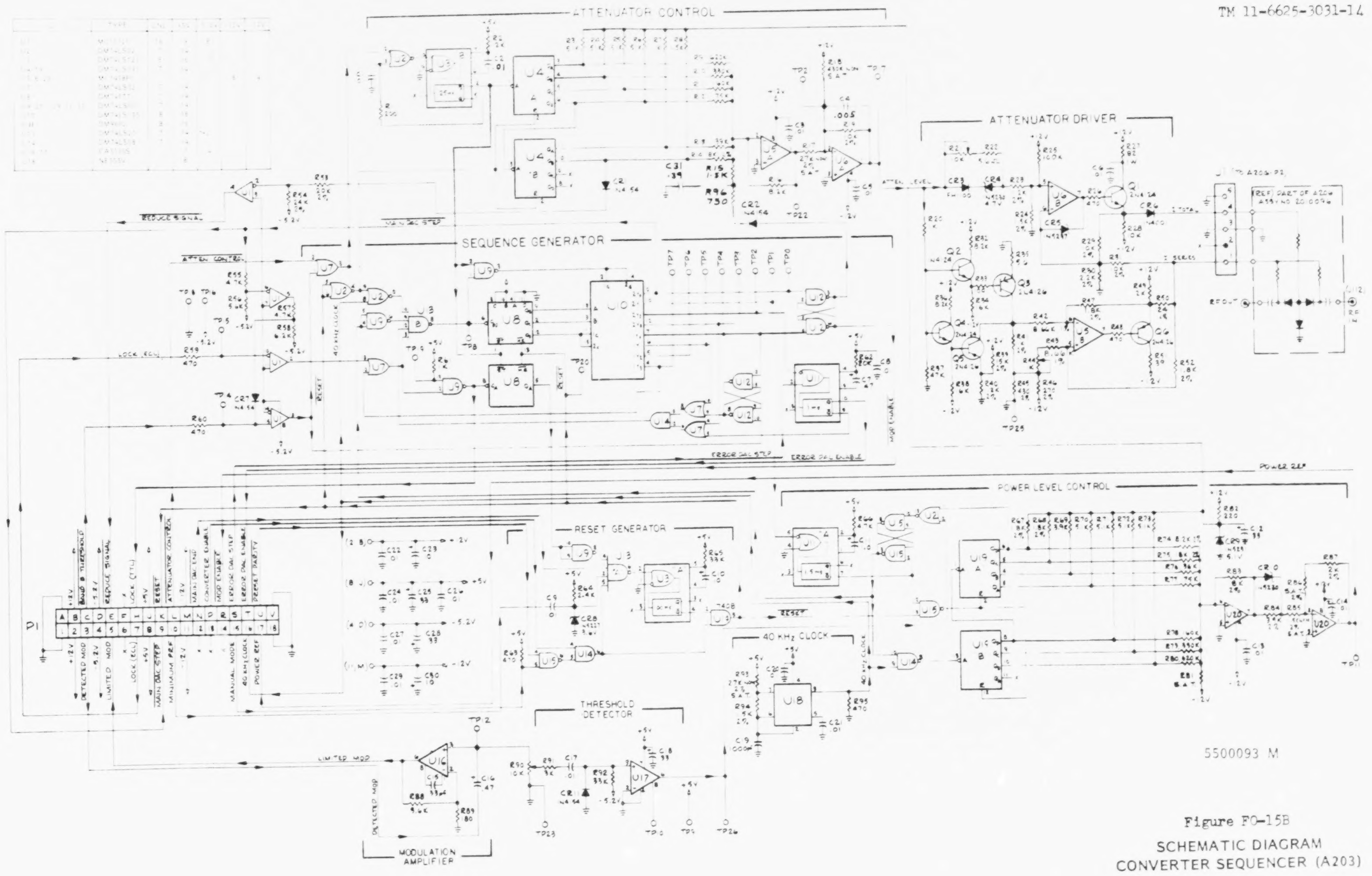
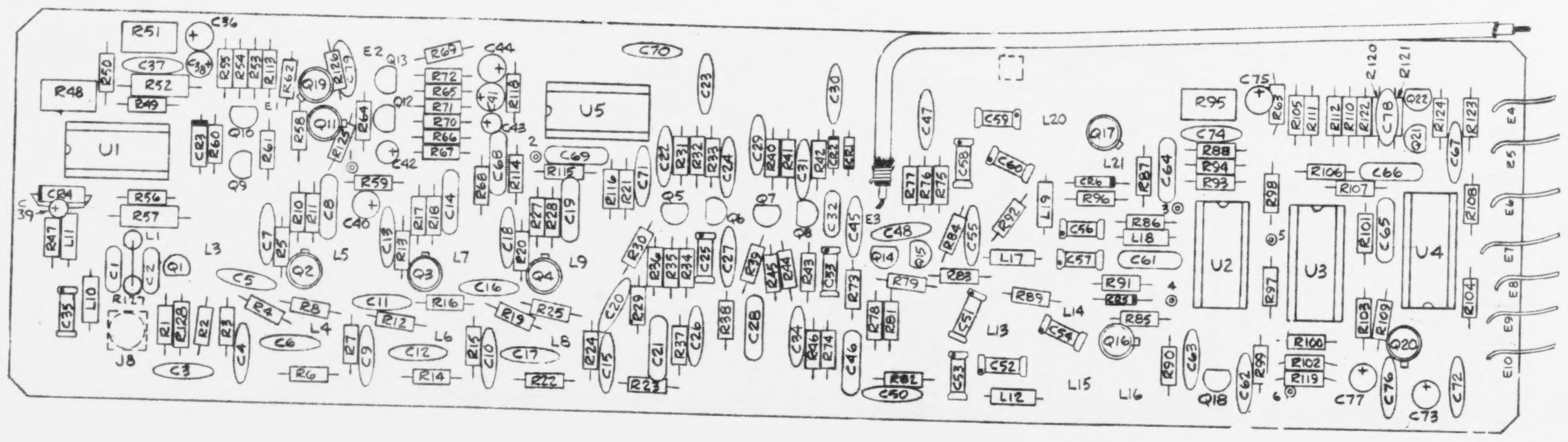

ATTENUATOR CONTROL
SEQUENCE GENERATOR
ATTENUATOR DRIVER
POWER LEVEL CONTROL
RESET GENERATOR
40 kHz CLOCK
THRESHOLD DETECTOR
MODULATION AMPLIFIER
P1
REDUCE SIGNAL
LIMITED MOD
DETECTED MOD
POWER REF
5500093 M

Figure FO-15B
SCHEMATIC DIAGRAM
CONVERTER SEQUENCER (A203)


R51
C36
C38
R50
C37
R52
R48
R49
R55
R54
R53
R113
R62
Q19
R126
C79
E2
Q13
R69
C44
R72
R65
R71
R70
R66
R67
C41
C43
R118
U5
C70
C23
C30
U1
CR3
R60
Q10
Q9
E1
R61
R58
Q11
R125
R64
Q12
C42
2
C69
C68
R114
R115
R68
CR4
C
39
R47
L11
R56
R57
L1
L3
C1
C2
Q1
R127
C35
L10
J8
R1
R128
R2
R3
C3
C4
C5
R4
R8
L4
C6
R6
C7
R5
R10
R11
C8
R59
C40
L5
Q2
C13
R13
R17
R18
C14
Q3
L7
C11
R16
R12
R7
C9
L6
C12
R14
R15
C10
C18
R20
R27
R28
C19
Q4
L9
C16
R19
R25
L8
C17
R22
R24
C15
R116
R21
C71
C22
R31
R32
R33
C24
Q5
Q6
C20
R29
R30
R36
R35
R34
C25
C27
R23
C21
R37
C26
R38
C28
C29
R40
R41
C31
R42
CR2
CR1
Q7
Q8
R39
R45
R44
R43
C33
C32
C34
R46
R74
R73
C45
E3
C48
Q14
Q15
C46
R78
R81
R82
C50
C47
R77
R76
R75
C58
R84
C55
R79
R83
C51
C53
L13
C52
L12
C59
L20
C60
R92
L17
L19
R89
C54
L14
Q17
L21
CR6
R96
C56
C57
R91
R85
R85
Q16
L15
L16
R87
C64
3
R86
L18
C61
4
R95
C75
C74
R88
R94
R93
U2
R90
C63
Q18
C62
R99
6
R63
R105
R111
R98
5
R97
U3
R100
R102
R119
R112
R110
R122
R120
R121
C78
Q22
Q21
R106
C66
R107
R101
C65
R103
R109
Q20
C77
C76
C73
U4
R124
C67
R123
R108
R104
C72
E4
E5
E6
E7
E8
E9
E10

2020094 N
9/78

## IF PROCESSOR (A204)

IF Processor A204 receives its input from the Mixer (A205). It separates the Mixer output into IF and Video components, and processes the components to produce several outputs. The IF signal is amplified and limited for counting. The Video signal is used to produce the SIGNAL THRESHOLD, DETECTED MODULATION, and ATTENUATOR CONTROL signals directly. SIGNAL THRESHOLD is combined with the external INHIBIT INPUT to produce BAND B THRESHOLD. This signal, together with the IF signal, is used to determine LOCK.

### IF Amplifier

The IF component of the Mixer output is amplified in a six stage amplifier having an overall gain of 50 dB, and a bandwidth covering 100 MHz to 375 MHz. Stage 1 (Q1) is a common emitter amplifier with shunt feedback (R2). L2 and L3 provide high frequency shaping of the response. Stages 2, 3, and 4 (Q2-4) are similar to Stage 1. Gain is set by the emitter resistors. High frequency gain shaping is provided by the emitter RC network (R11,C8), and the collector inductor (L5).

Stages 5 and 6 are limiting amplifiers, each consisting of an amplifier (Q5,Q7) and an emitter follower (Q6,Q8). Each stage has a nominal gain of 10 dB, determined by the input and feedback resistors (R30,34,35). Capacitive bypassing (C25) is used for high frequency gain shaping. Diodes (CR1,2) limit the final output still further.

### Video Circuits

The Video output of the Mixer, representing the detected envelope of a microwave signal, is amplified by U1. R48 sets the voltage gain (nominally 100), while R51 nulls out any offset between the differential outputs at U1 pins 7 and 8.

Outputs of U1 are applied to a high speed differential amplifier (Q9,10). Positive feedback from R61 converts this circuit to a Schmitt trigger. Q11 is an emitter follower used to drive the high speed ECL gates. The same outputs of U1 also differentially drive comparator U5 which forms the Attenuator Threshold Detector. Resistive biasing and feedback (R114-116,118) set the trigger level of this circuit approximately 7dB above the Signal Threshold Detector level.

The remaining Video circuit is the 20 kHz amplifier consisting of Q12 and Q13. This circuit provides an additional voltage gain of 100 at frequencies near 20 kHz, and is used to detect the modulated comb lines during YIG leveling and centering operations.

### In-Band Detector

The In-Band Detector determines whether or not an IF signal exists within the correct frequency range and at sufficient level to obtain LOCK. The correct frequency range is the region from 100 MHz to 325 MHz. After LOCK, the upper end of this region is extended to 350 MHz.

A portion of the IF signal is coupled into an additional limiter section (Q14,15) similar to the limiters in the IF Amplifier section. The output then drives two filter networks in parallel. The output of each network is detected (CR5,-CR6), and compared in U2. Since input signal amplitude is held constant, the detected signals are determined entirely by the filter characteristics. One of the filter networks consists of a 100 MHz high-pass section (C51-53,-L12) in series with a 325 MHz low-pass section (L13-16,-C54), thus forming a band-pass filter from 100-300 MHz.

The second network consists of a 100 MHz low-pass section (L17-19,C57) in parallel with a 325 MHz high-pass section (C58-60,L20,L21), forming a band reject filter from 100-325 MHz.

By comparing the outputs of these two networks in U2, a determination of the IF frequency is made. R95 is used to precisely set the crossover frequency. After LOCK is obtained, Q16 and Q17 are turned on, shorting out L16 and L21, and increasing the crossover point from 325 MHz to 350 MHz.

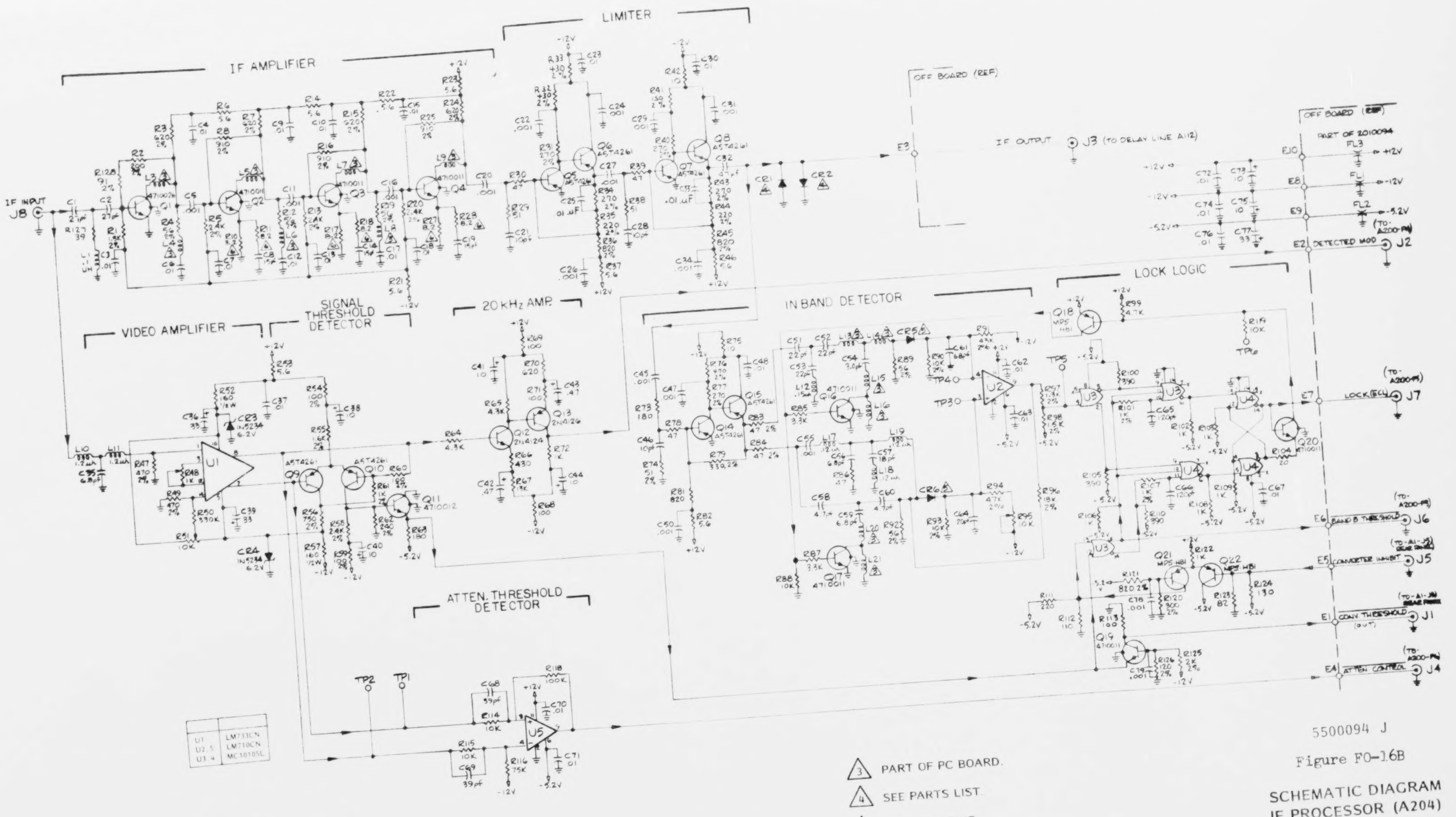
### LOCK Logic

The LOCK logic determines whether or not the proper conditions exist to consider the Converter locked. The condition to obtain LOCK is that an In-Band signal (from U2 pin 9) appears within 70 nanoseconds of the appearance of BAND B THRESHOLD (at Q11 collector). Once this condition is met, the LOCK command is latched, and remains active until a loss-of-lock condition is obtained — that is: an In-Band signal is not received within 70 nanoseconds of BAND B THRESHOLD.

BAND B THRESHOLD is generated by combining CONVERTER THRESHOLD (from Q11) with the external INHIBIT INPUT. The INHIBIT INPUT is buffered by Q21 and Q22. The two signals are combined at pins 12 and 13 of OR gate U3.

The LOCK latch consists of two gates of U4 with the output at U4 pin 14. The set input to this latch (U4 pin 5) is driven by a 3-input NOR gate (U4). The latch is set when all three inputs of the NOR gate are simultaneously low. R107 and C66 provide a 70 nanasecond delayed BAND B THRESHOLD to one input, while the inverted signal without a delay is applied to the second input. An inverted IN-BAND signal is applied to the third input. Thus a 70 nanosecond interval exists after BAND B THRESHOLD occurs, during which the LOCK latch may be set. The reset input to the latch is also a 3-input gate (U3), connected so IN-BAND must occur within 70 nanoseconds or the latch will be reset. If IN-BAND drops out while BAND B THRESHOLD remains (at any point in time after the 70 nanosecond interval), the latch is immediately reset.

Figure FO-16A
Component Locator
and
Descriptive Information
IF PROCESSOR (A204)


IF AMPLIFIER
LIMITER
IF INPUT
J8
OFF BOARD (REF)
IF OUTPUT
J3 (TO DELAY LINE A-11)
E3
OFF BOARD (REF)
E10
E8
E9
E2
+12V
-12V
-5.2V
DETECTED VIDEO
J2
VIDEO AMPLIFIER
SIGNAL THRESHOLD DETECTOR
20 kHz AMP
IN BAND DETECTOR
LOCK LOGIC
U1
U2
U3
U5
TP1
TP2
TP30
TP40
LOCK
J7
E7
E6
J6
E5
J5
E1
CONV THRESHOLD (OUT)
J1
E4
ATTEN CONTROL
J4
ATTEN THRESHOLD DETECTOR
U1
U2, 5
U3, 4
LM733CN
LM710CN
MC10105L

5500094 J

Figure FO-16B

SCHEMATIC DIAGRAM
IF PROCESSOR (A204)

3 PART OF PC BOARD.
4 SEE PARTS LIST.
5 MATCHED PAIR.